



**UNIVERSITAT POLITÈCNICA DE CATALUNYA  
BARCELONATECH**

**Departament d'Enginyeria Electrònica**

## **ANALYSIS OF THE HIGH FREQUENCY SUBSTRATE NOISE EFFECTS ON LC-VCOS**

Thesis submitted in partial fulfillment of the requirement for the PhD Degree issued by the Universitat Politècnica de Catalunya, in its Electronic Engineering Program.

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## RESUM

Anàlisi dels Efectes del Soroll de Substrat d'Alta Freqüència en Oscil·ladors LC

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La integració de transceptors per comunicacions de radiofreqüència en CMOS pot quedar seriosament limitada per la interacció entre els seus blocs, arribant a desaconsellar la utilització de un únic dau de silici. El soroll d'alta freqüència generat per certs blocs, com l'amplificador de potència, pot viatjar pel substrat i amenaçar el correcte funcionament de l'oscil·lador local. Trobem tres raons importants que mostren aquest risc d'interacció entre blocs i que justifiquen la necessitat d'un estudi profund per minimitzar-lo. Les característiques del substrat fan que el soroll d'alta freqüència es propagui més fàcilment que el de baixa freqüència. Per altra banda, les estructures de protecció perden eficiència a mesura que la freqüència augmenta. Finalment, el soroll d'alta freqüència que arriba a l'oscil·lador degrada al seu correcte comportament. El propòsit d'aquesta tesi és analitzar en profunditat la interacció entre el soroll d'alta freqüència que es propaga pel substrat i l'oscil·lador amb l'objectiu de poder predir, mitjançant un model, l'efecte que aquest soroll pot tenir sobre el correcte funcionament de l'oscil·lador. Es volen proporcionar diverses guies i normes a seguir que permeti als dissenyadors augmentar la robustesa dels oscil·ladors al soroll d'alta freqüència que viatja pel substrat.

La investigació de l'efecte del soroll de substrat en oscil·ladors s'ha iniciat des d'un punt de vista empíric, per una banda, analitzant la propagació de senyals a través del substrat i avaluant l'eficiència d'estructures per bloquejar aquesta propagació, i per altra, determinant l'efecte d'un to present en el substrat en un oscil·lador. Aquesta investigació ha mostrat que la injecció d'un to d'alta freqüència en el substrat es pot propagar fins arribar a l'oscil·lador i que, a causa del 'pulling' de freqüència, pot modular en freqüència la sortida de l'oscil·lador. A partir dels resultats de l'anàlisi empíric s'ha aportat un model matemàtic que permet predir l'efecte del soroll en l'oscil·lador. Aquest model té

el principal avantatge en el fet de que està basat en paràmetres físics de l'oscil·lador o del soroll, permetent determinar les mesures que un dissenyador pot prendre per augmentar la robustesa de l'oscil·lador així com les conseqüències que aquestes mesures tenen sobre el seu funcionament global (trade-offs). El model ha estat comparat tant amb simulacions com amb mesures reals demostrant ser molt precís a l'hora de predir l'efecte del soroll de substrat.

La utilitat del model com a eina de disseny s'ha demostrat en dos estudis. Primerament, les conclusions del model han estat aplicades en el procés de disseny d'un oscil·lador d'ultra baix consum a  $2.5\text{ GHz}$ , aconseguint un oscil·lador robust al soroll de substrat d'alta freqüència i amb característiques totalment compatibles amb els principals estàndards de comunicació en aquesta banda. Finalment, el model s'ha utilitzat com a eina d'anàlisi per avaluar la causa de les diferències, en termes de robustesa a soroll de substrat, mesurades en dos oscil·ladors a  $60\text{ GHz}$  amb dues diferents estratègies d'apantallament de l'inductor del tanc de ressonant, flotant en un cas i connectat a terra en l'altre. El model ha mostrat que les diferències en robustesa són causades per la millora en el factor de qualitat i en l'amplitud d'oscil·lació i no per un augment en l'aïllament entre tanc i substrat. Per altra banda, el model ha demostrat ser vàlid i molt precís inclús en aquest rang de freqüència tan extrem.

## ABSTRACT

Analysis of the High Frequency Substrate Noise Effects on LC-VCOs

by

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The integration of transceivers for RF communication in CMOS can be seriously limited by the interaction between their blocks, even advising against using a single silicon die. The high frequency noise generated by some of the blocks, like the power amplifier, can travel through the substrate, reaching the local oscillator and threatening its correct performance. Three important reasons can be stated that show the risk of the single die integration. Noise propagation is easier the higher the frequency. Moreover, the protection structures lose efficiency as the noise frequency increases. Finally, the high frequency noise that reaches the local oscillator degrades its performance. The purpose of this thesis is to deeply analyze the interaction between the high frequency substrate noise and the oscillator with the objective of being able to predict, thanks to a model, the effect that this noise may have over the correct behavior of the oscillator. We want to provide some guidelines to the designers to allow them to increase the robustness of the oscillator to high frequency substrate noise.

The investigation of the effect of the high frequency substrate noise on oscillators has started from an empirical point of view, on one hand, analyzing the noise propagation through the substrate and evaluating the efficiency of some structures to block this propagation, and on the other hand, determining the effect on an oscillator of a high frequency noise tone present in the substrate. This investigation has shown that the injection of a high frequency tone in the substrate can reach the oscillator and, due to a frequency pulling effect, it can modulate in frequency the output of the oscillator. Based on the results obtained during the empirical analysis, a mathematical model to predict the effect of the substrate noise on the oscillator has been provided. The main advantage of this model is the fact that it is based on physical parameters of the oscillator and of the noise, allowing to determine the measures that a designer can take to increase the robustness of the oscillator as well

as the consequences (trade-offs) that these measures have over its global performance. This model has been compared against both, simulations and real measurements, showing a very high accuracy to predict the effect of the high frequency substrate noise.

The usefulness of the presented model as a design tool has been demonstrated in two case studies. Firstly, the conclusions obtained from the model have been applied in the design of an ultra low power consumption  $2.5\text{ GHz}$  oscillator robust to the high frequency substrate noise with characteristics which make it compatible with the main communication standards in this frequency band. Finally, the model has been used as an analysis tool to evaluate the cause of the differences, in terms of performance degradation due to substrate noise, measured in two  $60\text{ GHz}$  oscillators with two different tank inductor shielding strategies, floating and grounded. The model has determined that the robustness differences are caused by the improvement in the tank quality factor and in the oscillation amplitude and not by an increased isolation between the tank and the substrate. The model has shown to be valid and very accurate even in these extreme frequency range.

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# Abbreviations

<b>AC</b>	Alternating Current
<b>BER</b>	Bit Error Rate
<b>CMOS</b>	Complementary Metal-Oxide Semiconductor
<b>CAD</b>	Computer Aided Design
<b>CML</b>	Current Mode Logic
<b>DC</b>	Direct Current
<b>EM</b>	Electromagnetics
<b>ED</b>	Electro Dynamic
<b>EQS</b>	Electro Quasy Static
<b>FDM</b>	Finite Difference Method
<b>HFSN</b>	High Frequency Substrate Noise
<b>HDMI</b>	High Definition Multimedia Interface
<b>IEEE</b>	Institute of Electrical and Electronics Engineers
<b>LNA</b>	Low Noise Amplifier
<b>mmW</b>	millimeter Wave
<b>NMOS</b>	Negative Metal-Oxide Semiconductor
<b>PGS</b>	Patterned Ground Shield
<b>PLL</b>	Phase Locked Loop
<b>PMOS</b>	Positive Metal-Oxide Semiconductor
<b>PA</b>	Power Amplifier
<b>PCB</b>	Printed Circuit Board
<b>QVCO</b>	Quadrature Voltage Controlled Oscillator
<b>RF</b>	Radio Frequency
<b>SNR</b>	Signal to Noise Ratio

<b>SiP</b>	System in Package
<b>SoC</b>	System on Chip
<b>WLAN</b>	Wireless Local Area Network

# Chapter 1

## Introduction.

### 1.1 Thesis scope and motivation

During the last years, the basic physical limits of the CMOS scaling are restricting the evolution trends of the CMOS integration. The Moore's Law is starting to be limited by the fact that reducing the size of a transistor does not necessary imply an improvement in terms of power consumption, size, performance and even price. The CMOS industry has been investing during the last years in the improvement of the system level integration as a path to continue with the improvement in cost, size and performance that the conventional CMOS scaling alone is not able to provide. The complete System-on-chip (SoC) IC integration (see Fig.1.1 left) is the main goal of nowadays semiconductors industry, which is always focused in "getting more functionality at an affordable cost", according to Rao Tummala [1], one of the main researchers about system integration.

Unfortunately, the "dreamed" situation of a complete SoC integration is presenting a lot of challenges and drawbacks. The integration of circuits or systems with very different characteristics, like mixed signal design, causes an increase in R+D cost and time to market, which limits the number of scenarios where SoC is really an optimum solution. System-in-Package (SiP) is a solution where two or more dies are integrated in the same package (see Fig.1.1 right), trying to deal with the before mentioned challenges [2]. SoC can be understood then as a special case of SiP where the number of dies is one. In Tables 1.1 and 1.2 [2] the main advantages and disadvantages of the division of a design into several silicon dies are shown. A reduced number of dies helps in terms of reliability, high-volume cost and general performance of the system. But other characteristics are worsened

when a reduced number of dies is used, as the reusability of IPs and the capability of upgrading individual components, both critical in shorting the so important time-to-market. In summary, in terms of just performances the best solution uses the minimum possible number of dies (being the SoC the ideal paradigm), but in systems where there is no high volume production or with tight time-to-market requirements the optimum number of dies increases. In any case, it is clear that the complete atomization of a design into a large number of dies is also far from being the best solution and a high effort should be done to cope with the few dies/SoC drawbacks.

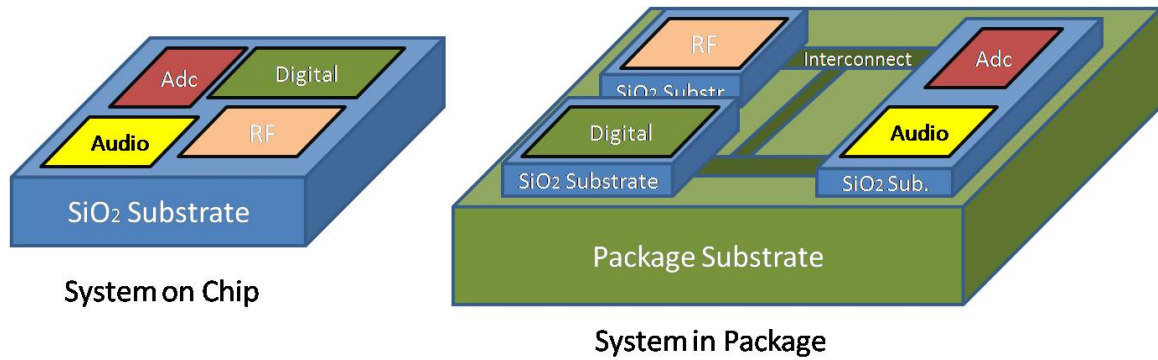


Figure 1.1. Typical SiC and SoP structures

One of the expanding fields in which the SoC paradigm has exploited its strengths and potential benefits, is the implementation of communication systems for portable applications. The integration of wireless radiofrequency transceivers –physical layer– together with data processing network management and data processing in the digital domain, all in a single silicon die, enabled low-cost, low-volume and low power solutions for communication systems that boosted the appearance of all kind of portable gadgets, the well known mobile revolution that started in the early 2000’s and that today keeps changing our daily life and the global economy.

The first SoC solutions appeared in the early 2000’s for low-demanding communication standards, like the SoC shown in Fig.1.2(a), implementing the Bluetooth V1.0 specification at a 1 *Mbps* rate, -80 *dBm* sensitivity and +2 *dBm* output power [3]. In subsequent years, SoCs for IEEE 802.11n WLAN communication standards ( [4], Fig. 1.2(b)), telephony ( [5], Fig.1.2(c)), or positioning ( [6], Fig.1.2(d)) were developed, achieving increasing performance in terms of data rate, sensitivity or transmitted power.

From the many challenges associated to the design of RF-communication SoC, one of the most critical issues is the electrical interaction between different blocks using the same silicon substrate, which can even force a SoC design to move into a SiP solution. Several authors have reported the

Market and Financial Issues		
Item	SiP	SoC
Relative NRE cost	1X	4X to 10X
Time to Market	3 to 6 months	6 to 24 months
Relative Unit Cost	1X	0.2X to 0.8X

Table 1.1. Market and Financial issues comparison between SiP and SoP

Technical Features	
Pros	
SiP	SoC
Can combine different front end technologies; GaAs, InP, Si, SiGe, etc.	Better yields at maturity (this depends upon complexity)
Can combine different device generations	Greater miniaturization
Re-use of common devices	Improved performance
Reduced size vs. conventional packaging	Lower cost in high volume
Active and passive devices can be embedded	CAD systems automate interconnect design
Individual components can be upgraded	Higher interconnect density
Better yields for smaller chip sets	Higher reliability (not true for very large die)
Individual chips can be redesigned cheaper	Simple logistics
Noise and crosstalk can be isolated better	
Cons	
SiP	SoC
More complex assembly	Difficult to change
More complex procurement and logistics	Product capabilities limited by chip technology selected
Power density for stacked die may be too high	Yields limited in very complex, large chips
Design Tools may not be adequate	High NRE cost
Signal integrity in interconnects	Noise interaction between blocks

Table 1.2. Technical features comparison between SiP and SoP

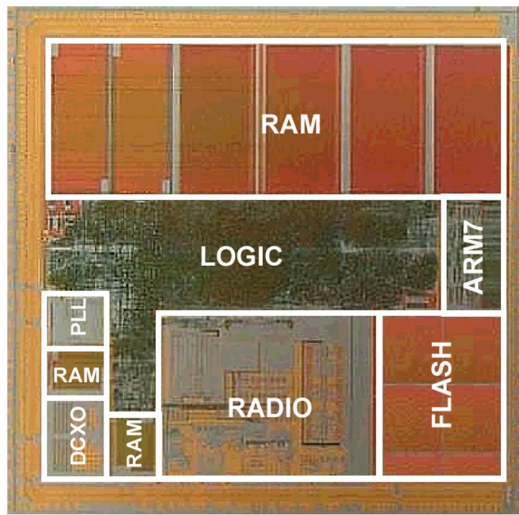
harmful effects that a digital block or a mixed-signal block can have over, for example, a delicate RF or Microwave receiver, where the digital switching noise propagated through the common silicon substrate can easily overwhelm the extremely low signals that are processed by the RF blocks for a minimum sensitivity.

One of the RF blocks that is very sensitive to the noise in the substrate is the Voltage Controlled Oscillator (VCO), that implements the local oscillator with channel-tuning capability, necessary in heterodyne and homodyne architectures. The presence of noise in the substrate can harm the VCO performance in terms of output spectral purity, phase noise and it can even modify the oscillation frequency, having an important impact in the correct behavior of the rest of the blocks connected to it and the overall system performance. It is important to note that not only the noise coming from a digital circuit can have an effect on the VCO. Other RF blocks of the same transceiver can play an important role in the noise injection on the substrate, like for example a Power Amplifier that will normally inject noise at a frequency very close to the VCO fundamental output frequency.

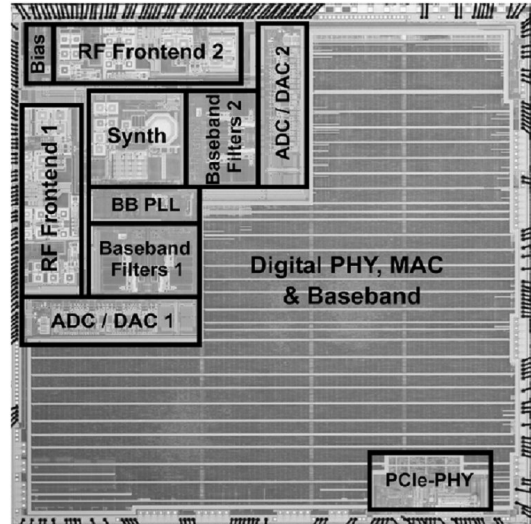
It is expected that problems caused by high frequency noise propagating through the substrate will worsen as the technology scales and frequencies exceed the RF range and enter the millimeter wave range (mmW). Capacitive couplings gain relevance and noise transmission through the substrate is easier, given the decreasing impedance of silicon at those frequencies [7]. Moreover, most of the typical measures to isolate the sensitive blocks from HFSN (High Frequency Substrate Noise) lose their efficacy or are difficult to implement in the millimeter band [8], [9].

It is well known that low frequency substrate noise is upconverted by RF VCOs and is manifested as sideband spurs at the VCO output. This effect has been extensively analyzed, as well as the efficacy of guard rings and other isolation structures to mitigate this VCO performance degradation [10]–[12]. However, a different phenomenon occurs when the substrate noise has a high frequency. Little work has been done on the robustness of VCOs to high frequency substrate noise or about the efficiency of shielding techniques in this frequency range.

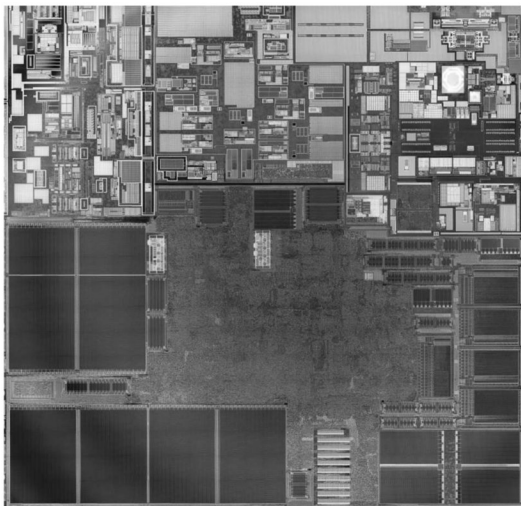




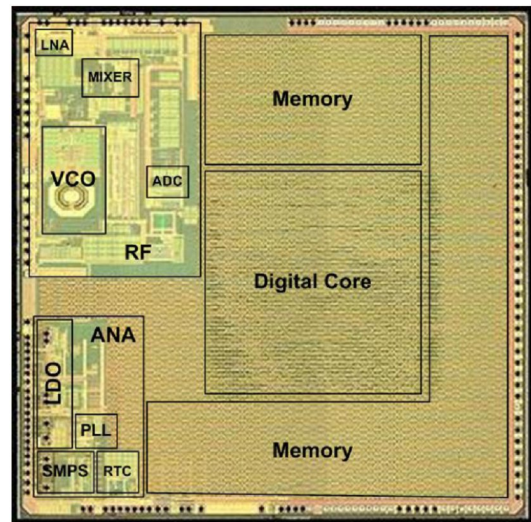
(a) SoC implementing the Bluetooth V1.0 specification [3].



(b) SoC implementing the IEEE 802.11n Wireless LAN specification [4].



(c) Single chip cellular radios for GSM, GPRS, EDGE implementation [5].



(d) GPS SoC implementation [6].

Figure 1.2. SoC implementation of different communication standards.

## 1.2 Thesis objectives

The main objective of this thesis is to provide designers with models, design criteria and methodology to design LC-VCOs robust to high frequency substrate noise. These methods and tools should be supported by a solid base, both from the empirical and theoretical point of view. The solutions provided to the designer need to be feasible and practicable and the trade off and consequences on the LC-VCO performance should be anticipated.

In order to define these methods that can efficiently reduce the effect that the high frequency substrate noise has on the VCO it is important to deeply analyze the following issues:

- Noise propagation: How does the noise propagate through the substrate?
- Effect of the HFSN on the oscillator and coupling mechanisms: Which is the effect of the noise on the performance of the oscillator? Which parameters of the noise and of the oscillator determine the level of performance degradation? Which are the main coupling mechanisms from the substrate to the VCO and which are the factors that determine the level of coupling (noise frequency, transistor dimensions, layout characteristics...)?
- Modeling the effect of HFSN on the LC-VCO: Is it possible to correctly model the effect of HFSN on the LC-VCO? Can this model be based on physical design parameters of the noise or of the LC-VCO (noise frequency/amplitude, transistor dimensions, layout characteristics...)? How accurate and which are the limitations of this model?
- Noise reduction methods and design rules: What kind of methods can be used to increase the isolation between the VCO and the main contributors to substrate noise? Which is the efficiency of these methods and for which noise frequency ranges? Which design rules should a VCO designer follow to create a noise robust VCO? Which are the consequences on the basic oscillator performance?

### 1.3 Thesis structure

This thesis will be structured in eight chapters. A preliminary literature review regarding the analyzed topic is introduced in chapter 2. This chapter will present the most relevant state-of-the-art relative to substrate noise on oscillators and design of protection structures. It will provide a starting point to the research phase of this thesis. The substrate propagation topic introduced in the literature review (chapter 2) will be deeply analyzed in Chapter 3, showing the results of two original performed studies. Firstly, it will be shown how the noise propagates through the substrate between two points up to  $40\text{ GHz}$  and the efficiency of some noise blocking or noise sinking structures to isolate the two points. Secondly, it will also be shown that inductors can be a high contributor to the injection and extraction of noise from the substrate. Chapter 4 will present an empirical analysis showing the real measurements performed to an LC-VCO affected by high frequency noise injected in the substrate. The LC-VCO - noise interaction will be described and the parameters that have a relevant effect will be empirically determined showing which of them can be critical to the oscillator performance. Chapter 5 will present an analytical justification of the observed phenomena and it will also develop an accurate model of the effect of HFSN on an LC-VCO, which agrees with the observations and conclusions of the measurements in Chapter 4. The model gives a very clear insight of the interaction between the HFSN and the LC-VCO. The individual analysis of each of the critical parameters shown by the model will make it possible to determine several methods to efficiently reduce the performance degradation of the LC-VCO due to HFSN. The consequences and trade offs of these methods will be analyzed in order to foresee the effect on the oscillator performance or characteristics (like, for example, power consumption or occupied area). Chapters 6 and 7 will present two case studies of how the model can be applied to design HFSN robust LC-VCOs. Chapter 6 will show the design of a  $2.5\text{ GHz}$  Quadrature VCO based on a  $5\text{ GHz}$  LC-VCO and a frequency divider. The model will be used to determine several techniques to maximize the robustness to HFSN. Chapter 7 will show that the model is a valid tool, even at millimeter wave frequencies, to analyze the effect of HFSN on a  $60\text{ GHz}$  LC-VCO.

## 1.4 Thesis contributions

The investigation phase of this thesis has led to the publication of several scientific papers in journals and international conferences. Those publications are listed here.

### Journals:

Marc Molina, Xavier Aragonès, Diego Mateo, José Luis González, **"Inductor shielding strategies to protect mmW LC-VCOs from high frequency substrate noise."**, Microelectronics Journal; vol. 44 issue 5, pp. 405–413 , May 2013.

M. Molina, D. Gomez, X. Aragonès, D. Mateo, and J. González, **"Design of a 2.5GHZ QVCO robust against high frequency substrate noise."** Microwave and Optical Technology Letters, vol. 53, no. 7, pp. 1632–1637, July 2011.

### International conferences:

M. Molina, X. Aragonès, D. Mateo, and J. Gonzalez, **"Effect of high frequency substrate noise on LC-VCOs."** in Circuits and Systems (MWSCAS), 2010 53rd IEEE International Midwest Symposium on, pp. 157–160, aug. 2010. **Awarded one of the best 10 student papers in the conference.**

J. González, X. Aragonès, M. Molina, B. Martineau, and D. Belot, **"A comparison between grounded and floating shield inductors for mmW VCOs."**, ESSCIRC, 2010 Proceedings of the, pp. 250–253, sept. 2010.

M. Molina, X. Aragonès, J.L. González, **"Experimental analysis of substrate isolation techniques for RF-SOC integration."**, SOC Conference, 2009. IEEE International, pp. 199–202, sept. 2009.

Marc Molina, Didac Gómez, José Luis González, Diego Mateo, Xavier Aragonès, **"Ultra low power QVCO for the 2.5 GHz ISM band using a 5GHz LC VCO with a frequency divider."**, XXIII Design of Circuits and Integrated Systems Conference, pp. 1-6. Grenoble (France), November 2008.

Marc Molina, Xavier Aragonés, A. Goñi-Iturri y B. González, **"Modeling and experimental characterization of EM coupling between integrated spiral inductors."**, XXII Design Circuits and Integrated Systems Conference, pp. 65-70, Sevilla (Spain), November 2007.

## Chapter 2

# Review of previous work on substrate noise and its effect on LC-VCOs.

### 2.1 Substrate propagation and substrate modeling

During the last decade, high resistivity substrate has become a standard for RF-CMOS processes due to, among other issues, the possibility to integrate high quality passives required for RF applications and the reduced noise transmission. The analysis of the noise propagation on a high resistivity substrate presents much more complexity than in a low resistive substrate with a high resistive epitaxial layer, where the substrate can be simplified to as single electrical node [13]–[16]. In a high resistivity substrate, the noise currents are distributed through the whole volume of the substrate, not only in the surface, increasing the complexity of the propagation models. In order to properly simulate the effect that the substrate noise can have over a victim block, it is necessary to include the substrate model in the circuit level simulation. To obtain a reliable model of the noise propagation between different parts of the circuit and to guarantee the proper circuit level simulator integration, the substrate model must have a port for every substrate place where noise can be injected by an aggressor and for every single place where noise can couple to a victim.

Several methods can be used to obtain an equivalent model of the substrate between the ports. One of the common solutions uses FDM (finite difference model) approach to treat the substrate as a 3-D mesh where each cell in the mesh is modeled by a group of lumped elements [17], [18] consisting of a parallel combination of a resistor and a capacitor [19], [20], as shown in fig.2.1. In order to

reduce the complexity of the model obtained, the generated RC network should be approximated by a smaller circuit that exhibits equivalent electrical behavior. The reduction process has to guarantee that the reduced model retains the accuracy of the original model but containing orders of magnitude fewer circuit nodes [19], [21].

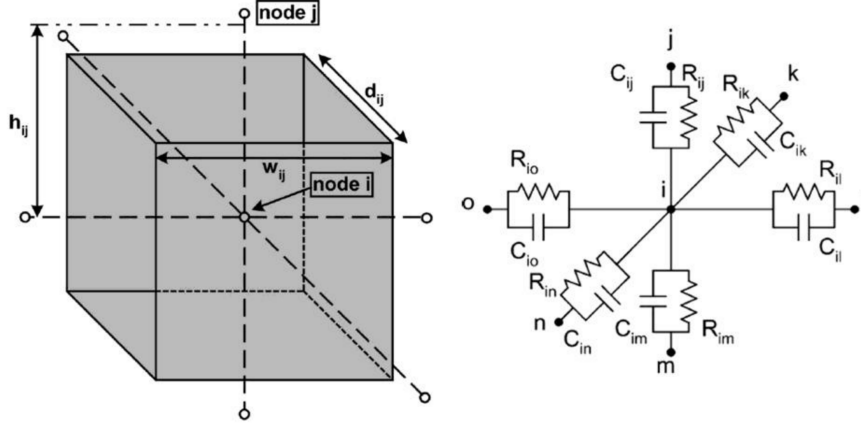


Figure 2.1. Substrate modeled as a collection of square cubes (left). Resistances and capacitances around a mesh node (right) [19].

The complexity of the network can be further simplified in those designs where the intrinsic capacitance of the substrate can be ignored, which is a reasonable assumption for operating frequencies of up to a few gigahertz and switching times less than about  $100\text{ ps}$ . In this case, the 3-D resistive mesh can be reduced to an equivalent set of  $n \cdot (n + 1)/2$  resistances interconnecting the  $n$  ports [22], [23]. A different approach to model the substrate consists in the use of the Green's equations [24] to obtain an analytical expression to model the impedance between the  $n$  ports instead of discretizing the whole structure. This method ends up with a much simpler matrix that can also be treated by a reduction process or can be modeled using lumped elements.

Both the FDM and Green equation approaches have been used to develop commercial substrate extraction tools<sup>1</sup> that are now commonly used to obtain models of the substrate parasitics to be included in post-layout simulations. Substrate extraction tools provide a convenient way to evaluate interactions between components in circuits with reduced number of elements, such as the interactions between different circuit blocks in a RF transceiver. When the substrate noise is produced by the activity of digital circuits, the problem is then the estimation of such generated noise, as well as

<sup>1</sup>Pioneering tools were SubstrateStorm and SeismIC, which were included in the Cadence design environment first with the name Assura RCX-HF, and now with the name Quantus QRC. ([http://www.cadence.com/products/di/quantus\\_qrc\\_extraction/pages/default.aspx](http://www.cadence.com/products/di/quantus_qrc_extraction/pages/default.aspx)). Other commercial tools for substrate coupling evaluation are WaveIntegrity from Coupling Waves Solutions (<http://www.cwseda.com/>) and SPX from Magwel (<http://www.magwel.com/>).

the huge number of ports required in the substrate model. In those cases, given the analog nature of the electrical noise, an analog simulation of the complete digital circuitry -as well as package and power distribution parasitics, to evaluate SSN- is ideally required, with ports at each of the components and contacts that interact with the substrate. Since such simulation is usually unfeasible even with fast-spice simulators, several macro-modeling methodologies have been developed in the last decade [25]–[27] in order to efficiently estimate the substrate noise from the generation side in digital circuits.

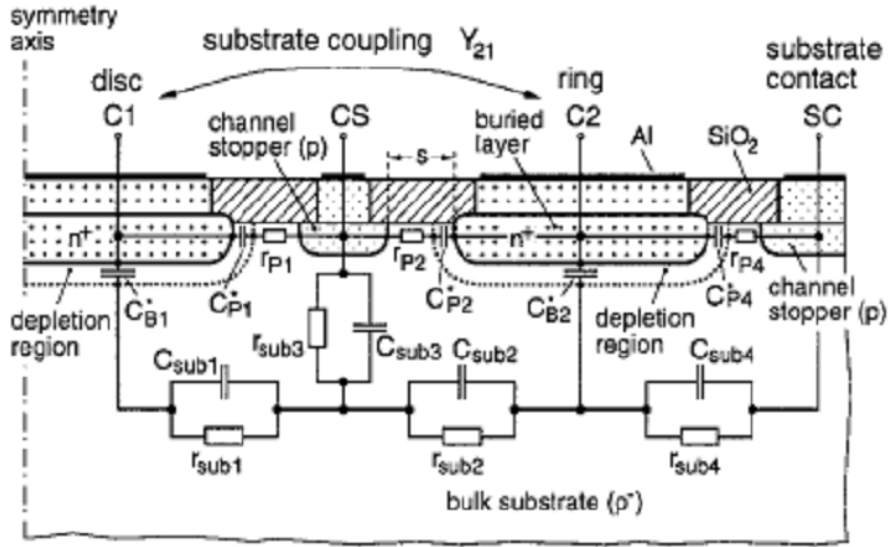


Figure 2.2. Cross section of a test structure with RC equivalent circuit for modeling substrate coupling [20]

These lumped element models provide a very comprehensive way to model the substrate but are limited to model the interaction between the ports. When some information regarding current distribution or voltage potential inside the substrate is required, 3-D electromagnetic simulators like HFSS [28], momentum [29] or IE3D [30] should be used.

The validity of these substrate models may degrade as signal frequencies scale up, since the range of validity of the electroquasistatic (EQS) models, like passive networks, is limited up to frequencies for which that distances of the substrate interactions are a small fraction of the wavelength. Particularly, [31] shows the limitation for the case of lightly doped processes, with non negligible levels of substrate-induced noise present within distances of up to  $500\ \mu m$ . As shown in Fig.2.3, a quasi-static model becomes inadequate when noise contains significant harmonics above  $30\ GHz$ , assuming typical substrate conductivities ( $\sigma \approx 1-10\ S/m$ ) and thicknesses ( $h \approx 200-300\ \mu m$ ), due to

the manifestation of surface waves characteristics. For extremely high frequencies, around millimeter wave, some authors propose some electrodynamic (ED) methods to model the substrate [32]–[34] based on Poisson’s and Green’s equations.

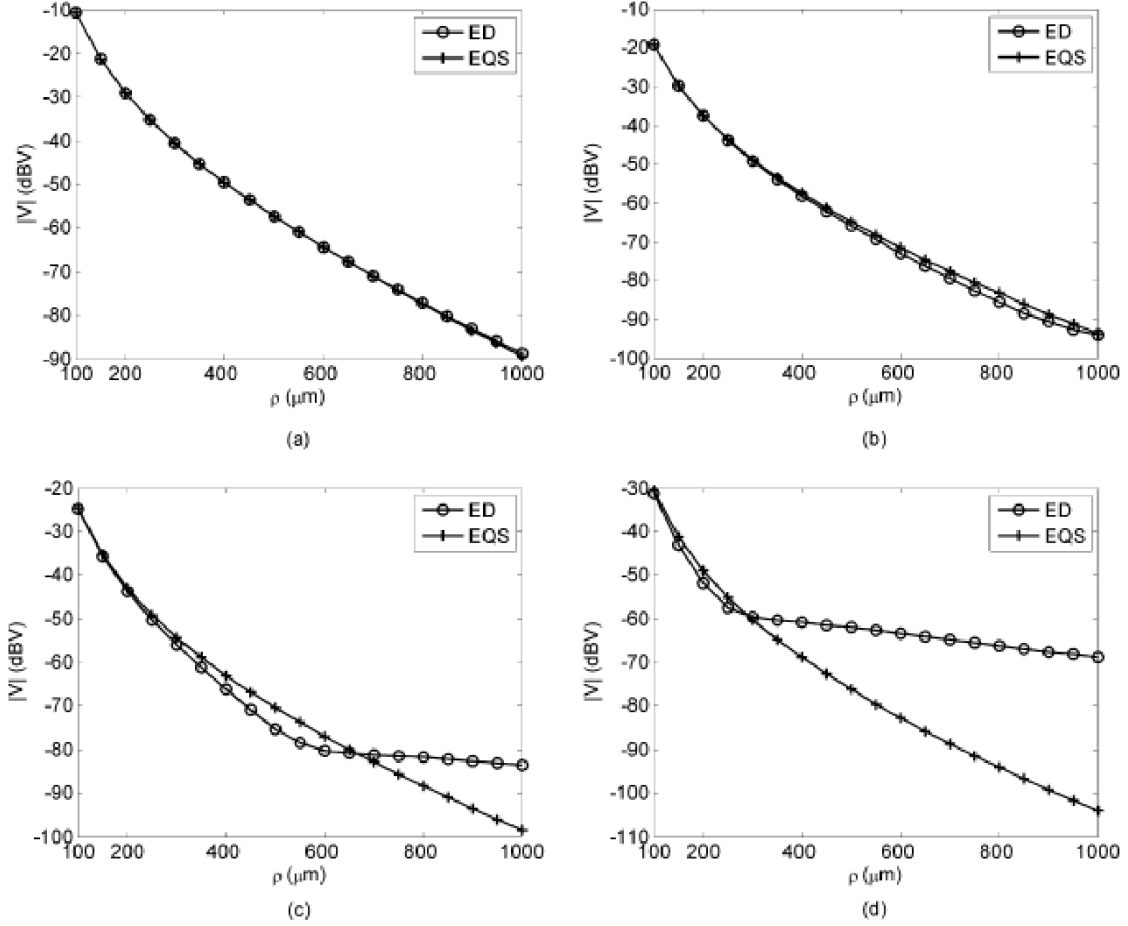


Figure 2.3. Voltage magnitudes from the ED and EQS computations at four different frequencies. (a)  $f = 2 \text{ GHz}$  (b)  $f = 15 \text{ GHz}$  (c)  $f = 30 \text{ GHz}$  (d)  $f = 60 \text{ GHz}$  [31].

## 2.2 Effect of substrate noise on LC-VCOs

LC-VCO are one of the most sensitive analog circuits to the harmful effects of noise generated by other analog blocks or by the switching of digital circuits residing on a common substrate. The effect of the substrate noise on the output spectrum of a VCO has been usually analyzed from two different perspectives. A realistic approach to evaluate digital substrate noise consists in the analysis of a victim VCO placed close to a digital circuit that generates realistic switching noise [10]. This approach provides a realistic case study but the complexity of the switching noise spectrum makes it difficult to distinguish which is the source of each of the effects observed on the VCO output.



A more academic approach consist in the injection of a pure tone through a pad connected to the substrate [10], [11], [35], [36]. This kind of analysis makes it easier to evaluate the cause-effect relationship between the injected noise and the VCO impact, allowing the isolation and evaluation of the coupling mechanisms. This approach also imitates realistically the effect that other RF blocks integrated in the same die, like a power amplifier, can have on the VCO.

This section will review previous works that analyze the effect on VCOs of substrate noise generated by three different sources: digital switching noise, low frequency analog noise and high frequency analog noise.

### 2.2.1 Effect of digital switching noise on LC-VCO performance

The characteristics of the injected noise into the substrate have a high dependence with the switching characteristics of the digital blocks [35], [37], [38], like for example, switching frequency, switching slope or synchronization. Fig.2.4 shows the substrate injected noise spectrum generated by a digital circuit for two clock frequencies and compares it with the noise floor measured when the digital circuit is not enabled. In this figure, the two terms of the noise spectrum can be clearly observed: a train of impulses at multiples of the clock frequency and a continuous component. The continuous component of the noise is caused by the random component of the digital switching and its amplitude grows with the clock frequency. Fig.2.5 shows how the impact of this continuous term coupled to the VCO severely degrades its phase noise by more than 10 *dB*s on the complete range of frequencies. This effect worsens as the digital clock frequency is increased.

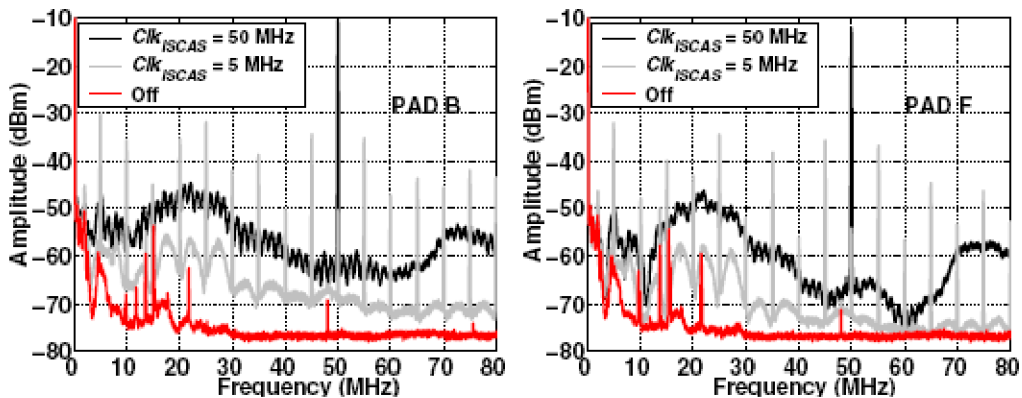


Figure 2.4. Noise generated at the digital ground (pad B) and substrate noise measured at the vicinity of the VCO (pad F) [35].

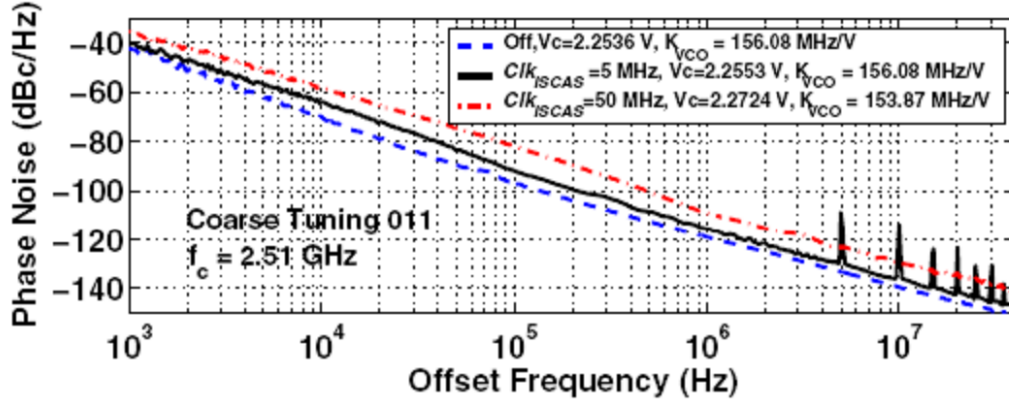


Figure 2.5. Experimental results of the measurement of the impact of digital substrate noise on the VCO [35].

Fig.2.5 also shows some spurs in the degraded phase noise. The same effect is also shown in Fig.2.6, which shows another example for a clock frequency on the digital block  $f_{clk} = 10\text{ MHz}$ . Many spurs appear around the oscillator fundamental frequency. These spurs are caused by the substrate noise coupled to the different parts of the LC-VCO, like the analog ground, the VCO active devices and passives local substrate nodes. The various spurs appearing in Fig.2.6 are labeled according to its origin. Group B come from low frequency substrate noise harmonics up-converted from close to DC to close to the VCO output frequency due to indirect AM to FM modulation. Group A and group C come from high frequency substrate noise harmonics converted from around the VCO fundamental frequency to phase noise sidebands.

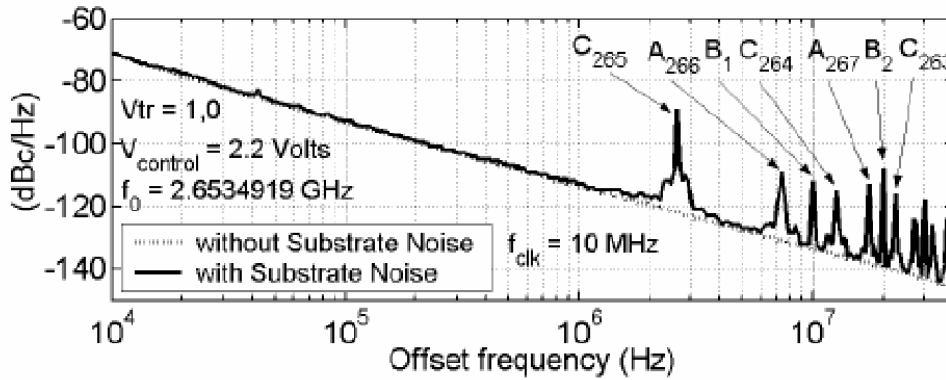


Figure 2.6. Effect of the substrate injected digital noise on the VCO Phase Noise [10].

The degradation of the phase noise of the VCO can affect the performance of the rest of the components connected to it. In RF transceivers, the VCO is typically found inside a frequency synthesizer or PLL. The consequences of the degradation of the VCO phase noise, due to the substrate

noise, on the performance of a PLL are analyzed in [39]–[42]. Fig.2.7 shows how the substrate noise can impact the jitter of the PLL due to the VCO phase noise degradation. It is obvious that the degraded phase noise of the VCO and the increased jitter of the PLL will have a direct effect on the performance of the complete system reducing SNR or increasing the BER.

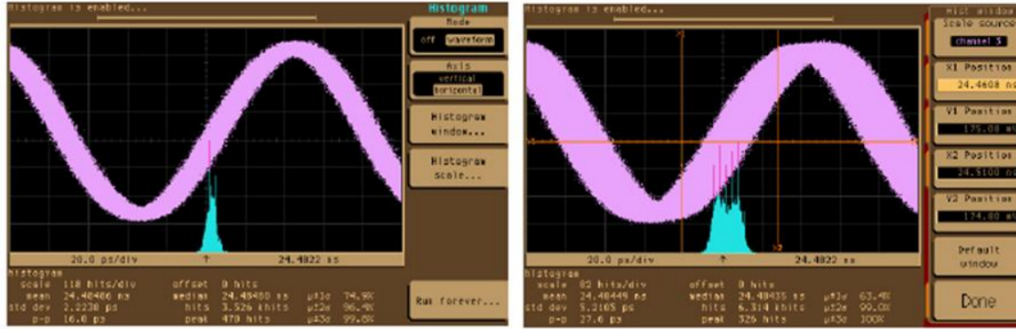


Figure 2.7. Demonstration that substrate noise generates PLL jitter. Left: PLL output with no substrate noise applied. Right: PLL output with substrate noise applied [39].

### 2.2.2 Effect on the LC-VCO performance of a low frequency tone in the substrate

The consequences of the injection of a low frequency single tone in the substrate have been widely analyzed [10], [11], [35], [36]. All these analysis show how the coupling of this tone into the VCO generates two sidebands around the fundamental VCO output frequency, see Fig.2.8. The offset frequency of the sidebands is determined by the frequency of the tone and it is independent of the oscillation frequency. The amplitude of the sidebands is determined by several factors, like the coupling mechanisms, the distance between the aggressor and the victim or the amplitude and frequency of the tone. The analysis of the amplitude can help to determine the coupling paths of the noise to the VCO.

The two sidebands are caused by the frequency modulation of the VCO output signal due to the noise [43]. Noise couples through several ways into the VCO tank and changes the DC operating point of the tank, changing the voltage across the varactor that controls the oscillating frequency and consequently changing the oscillation frequency at the rate of the noise.

There are several different options for the noise to reach the oscillator from the substrate [36]:

- Capacitive and inductive coupling to the inductor.

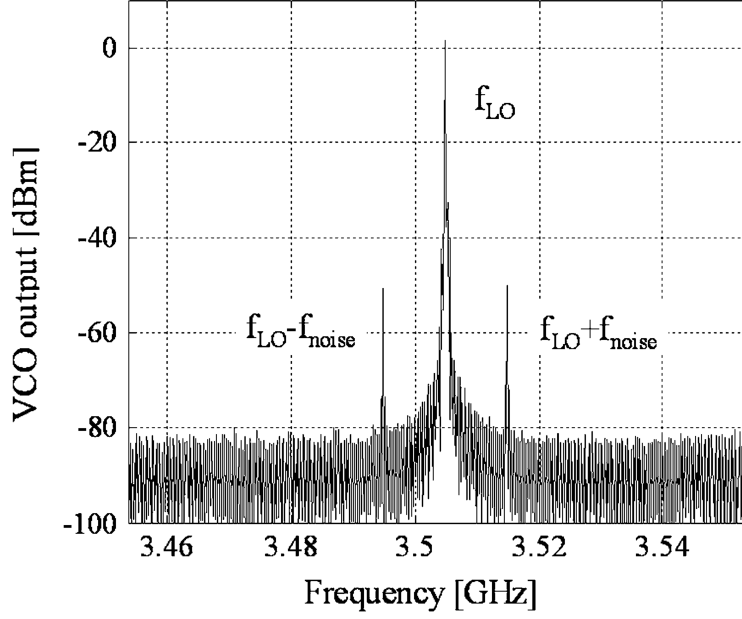


Figure 2.8. VCO output spectrum with spurious tones due to 15 dBm, 5 MHz noise tone [36].

- Capacitively through the n-well of the accumulation mode n-MOS varactor, to the varactor bulk node.
- Coupling to the backgates of the transistors. Resistively to the n-MOS transistor and capacitively through the n-well to the p-MOS transistor.
- Resistively and capacitively coupling to the non-ideal metal ground lines or ground planes.

Each of these coupling mechanisms can contribute to the LC-VCO degradation but there is a second very relevant term in this contribution, the level of sensitivity of the LC-VCO to each coupling mechanism. For example, a very low amplitude noise signal in one node may degrade the LC-VCO much more than a high amplitude noise signal in a different node.

When a sinusoidal substrate noise signal of amplitude  $A_{noise}$  and frequency  $f_{noise}$  reaches the oscillator, the output signal is modulated in frequency [12], [44]. The output voltage can be expressed as:

$$V_{out}(t) = A_{LO} \cdot \cos \left( 2\pi f_{LO}t + 2\pi \sum_i^n K_i(v_{tune}) \int_0^t (h_{sub}^i \cdot V_{sub})(t)dt \right) \quad (2.1)$$

where  $A_{LO}$  represents the oscillator amplitude and  $K_i$  the sensitivity of the oscillator frequency to a voltage variation  $V_i$ .  $n$  is the number of paths via which the substrate noise can enter the VCO.

$h_{sub}^i$  is the transfer function from the point where substrate noise originates, to the reception point  $i$  in the VCO.  $V_{sub}$  represents the sinusoidal noise signal traveling through the substrate.

Since the substrate noise signals are small compared to the local oscillator signal, narrow-band FM can be assumed and the expression for the amplitude of the sidebands tones at the VCO output becomes [44]:

$$|V_{out}(f_c \pm f_{noise})| = \left| \sum_i^n H_{sub}^i(f_{noise}) K_i(V_{tune}) \frac{A_c A_{noise}}{2f_{noise}} \right| \quad (2.2)$$

Experimental results [12], [35] have shown that the coupling to the inductor and the coupling to the ground are the two most relevant coupling mechanisms between the substrate and the LC-VCO due to their high sensitivity and high coupling from the substrate. Equation (2.2) can then be simplified to these two components.

$$|V_{out}(f_c \pm f_{noise})| = \left| \frac{A_c A_{noise}}{2f_{noise}} \left[ H_{sub}^{Gnd}(f_{noise}) K_{Gnd}(V_{tune}) + H_{sub}^{Ind}(f_{noise}) K_{Ind}(V_{tune}) \right] \right| \quad (2.3)$$

Several investigations have been carried out to analyze, simulate and define the effect and coupling paths of low frequency noise into the VCO. It has been widely agreed [12], [36], [43], [45] that the non ideal ground is one of the main paths between the VCO and the substrate. When the noise in the substrate reaches the ground of the circuit, it can create ground bounce due to the parasitic resistance of the GND metal as well as the bonding and package parasitic inductance. This effect is presented in [36], where the coupling of the noise to the ground power lines is analyzed as one of the main contributor to the VCO performance degradation. The author introduces a  $3.5\text{ GHz}$  VCO with the possibility of injecting a noise tone directly into the substrate. The VCO performance is analyzed in the noise frequency range from DC to  $15\text{ MHz}$ , showing the impact of the resistive coupling of noise from the substrate to the non-ideal on-chip ground interconnect, resulting in analog ground bounce and frequency modulation.

The main drawback of the experimental analysis presented in [36] is the limited frequency range of the noisy signal, which prevents observing other paths in which the noise couples capacitively to the VCO. This is the case of the coupling to the large-area spiral inductors (second term in expression (2.3)). This limitation has been overcome by later works [35], [46] in which similar measurements for a broader frequency range are presented. Fig.2.9 shows a  $1/f$  dependence of the spur amplitude vs. the noise frequencies up to a few tens of MHz, and after that the amplitude becomes frequency-

independent. The inversely proportional relation between spur amplitude and the substrate noise frequency proves that this is resulting from a resistive coupling (flat in frequency) followed by frequency modulation ( $-20$  dB/dec). At large frequencies, the capacitive mechanisms become relevant enough and dominate over the resistive ones. As the frequency-proportionality of the capacitive coupling compensates the  $1/f$  of the frequency modulation, the spur amplitude appears now constant versus the noise frequency.

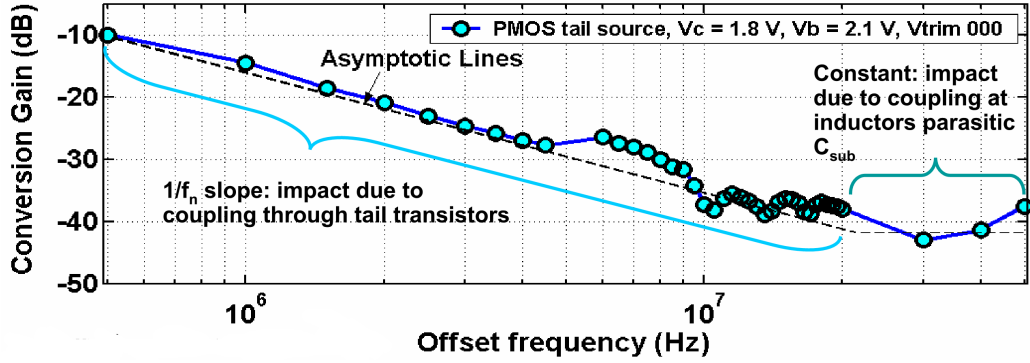


Figure 2.9.  $1/f$  dependence of the spur amplitude vs. the noise frequencies [35].

Experimental analysis provides a limited insight into the coupling mechanisms. Understanding with precision the main paths of coupling is essential to the circuit designer in order to undertake measures (adding isolation around specific components, for example) in order to minimize noise impact on the VCO output. Later works have combined experimentation, simulation and circuit analysis in order to provide this identification [12], [35], [44], [46]. In [36], a VCO including a realistic model of the ground network is simulated with the objective of determining the contribution of each of the coupling mechanisms. In this case, only resistive ground connections, NMOS transistor bulk and capacitive coupling to the inductor are analyzed. Fig.2.10 is a graphical representation of the simulation method showing, the substrate noise propagation, the coupling mechanisms taken into account and the interconnect metal network.

Fig.2.11 shows the contribution to the overall impact of the separate components in the investigated frequency range to the VCO performance in terms of sideband amplitude as a function of the noise frequency [46]. The dominant contribution is clearly coming from the non-ideal on-chip ground interconnect. Substrate noise couples resistively to the analog ground interconnect (via the substrate ties). Ground bouncing causes the voltage over the variable circuit capacitances (NMOS and PMOS capacitance, accumulation mode NMOS varactor capacitance) to vary, which results in

modulation of the local oscillator frequency. Impact via the inductor is significantly lower because it results from capacitive coupling which is negligible for the studied substrate noise frequencies. Impact via the NMOS back-gate is also inversely proportional to the noise frequency but small compared to the impact via the non-ideal ground interconnect .

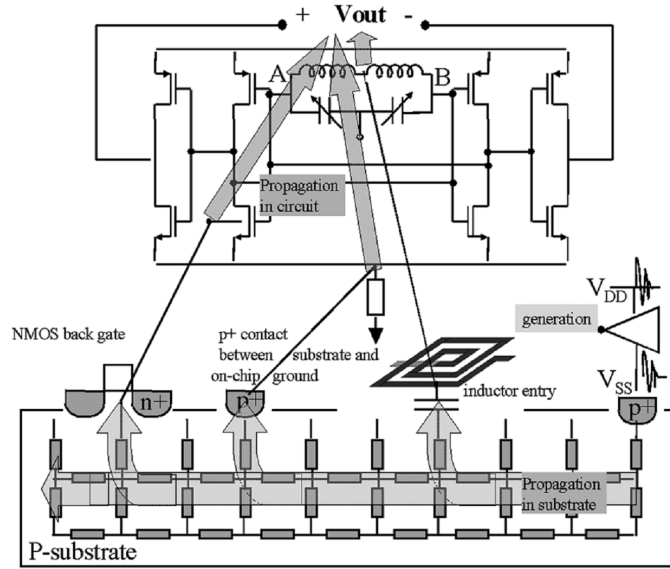


Figure 2.10. Presented simulation method to allow the analysis of impact of the substrate noise through the different components in the RF circuit [46].

While the works cited so far analyze the coupling mechanisms and effects in VCOs working in the few GHz range, particular attention must be paid to designs aimed for mm-Wave communications. Here, the increased frequency worsens the interaction problems between the different subsystems, making SoC integration of a complete transceiver very hard (although a SiP solution may be even harder due to long interconnections between dies). Moreover, passives are typically scaled down, which together with the use of alternative implementations (like transmission lines), may modify the noise coupling paths or the VCO sensitivity to substrate noise. Last, the simulation approaches based on lumped models of the substrate prove to be inadequate at these frequencies. The works dealing with the effects of the substrate noise on mm-wave VCOs are very limited. In [45] it is shown how, similar to the effect on lower frequency oscillators, sidebands appear around the fundamental oscillation frequency with a frequency offset equal to the noise frequency. This effect is proven experimentally in a 48-53 GHz LC-VCO designed in a UMC 0.13  $\mu m$  technology. The objective of this work is to find the dominant substrate noise entry points and predict the impact on the mmW VCO performance. Due to the extremely high frequency of the mmW VCO, the passive network substrate model does not provide enough accuracy and a 3D electromagnetic simulator (HFSS [28]) is

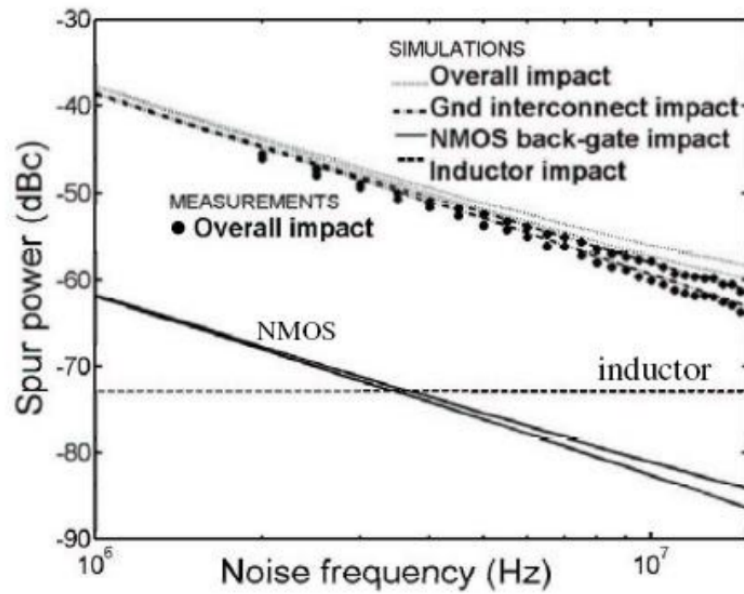


Figure 2.11. Contribution to the spur amplitude of each of the coupling mechanisms [46]

used to model the on-chip interconnects, the substrate and the passive components. Noise is injected at low frequency, from DC to  $500\text{ MHz}$ . Simulation results show how, again, the ground bounce is the dominant coupling mechanisms for low noise frequency. Fig.2.12 shows the HFSS simulated electrical fields at  $100\text{ MHz}$  and a comparison of the spur amplitude between real and ideal ground, evidencing the importance of modeling the GND and power parasitics. The main drawback of this analysis is the limited frequency of the noise signal. It would be very interesting to see how the different coupling mechanisms change for higher noise frequencies.

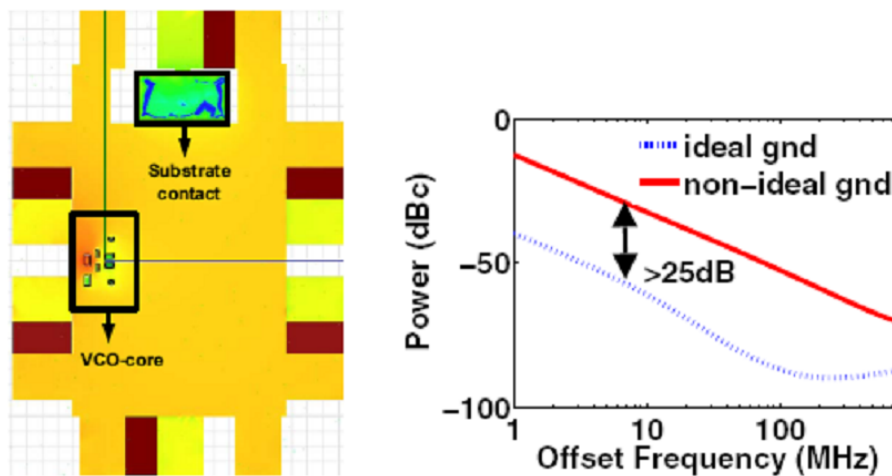


Figure 2.12. Electrical fields in the layout at  $100\text{ MHz}$  (left). Comparison of the sideband amplitude between ohmic and ideal ground [45].



As a summary, low frequency analog noise traveling through the substrate degrades the performance of LC-VCO due to the coupling of this noise into the sensitive nodes of the LC-VCO. The cause of performance degradation is generally attributed by most authors to the ground bounce in the LC-VCO caused by the substrate noise. Low frequency ground bounce changes voltage across the oscillator varactor changing the oscillator frequency. As the frequency of the noise increases, the varactor can't follow the rapid voltage changes and so, the interaction between the substrate noise and the LC-VCO should necessarily change.

### **2.2.3 Effect on the LC-VCO performance of a high frequency tone on the substrate**

Several characteristics of the effect of substrate noise on LC-VCOs change as the frequency of the noise increases. The capacitive behavior of the substrate makes the substrate impedance lower at high frequency, allowing the noise to flow easily through it and so, reaching the victim with higher power. The substrate models become more complex and the validity of the passive network propagation models needs to be reviewed. Moreover, high frequency noise can couple capacitively from the substrate into the oscillator. A physical connection is not required and so, the analysis of the coupling paths becomes much more complex. The effects of the high frequency noise on the LC-VCO should differ from those at low frequency, as, for example, the high frequency noise cannot change the biasing DC point of the varactor. Finally, the efficiency at high frequency of the isolation techniques used for low frequency isolation is still to be confirmed. A deep analysis is required to find the difference between low and high frequency substrate noise effect.

Again, experimentation is a good tool to cope with the limitations of simulation techniques at high frequency. The output spectrum of a  $900\text{ MHz}$  LC-VCO when a sinusoidal signal with a frequency of  $304\text{ MHz}$  is injected into the substrate is shown in Fig. 2.13 [47]. Several sidebands, caused by the effect of the noise, appear at different frequencies.

Both the effect on the LC-VCO as well as the coupling mechanisms have a very strong dependence with the frequency of the noise. The noise effect on the oscillator can be reviewed by measurements but identifying coupling mechanisms and paths requires advanced simulations.

After simulating the circuit together with the models of the substrate, interconnects and PCB, the authors of [47] conclude that the impact mechanism for this VCO can be divided into four frequency regions:

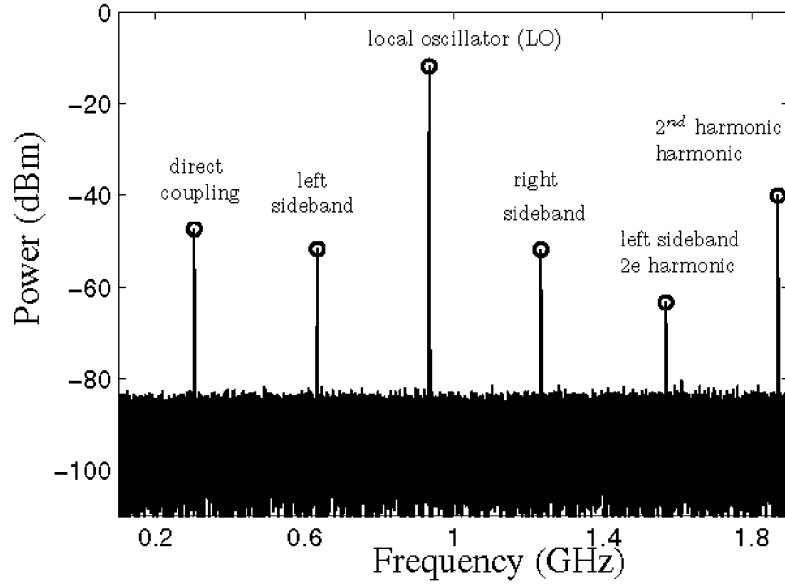


Figure 2.13. Output spectrum of a 900 MHz LC-VCO with a 304 MHz frequency interference injected into the substrate [47].

- At low frequencies, sideband spurs are caused by FM modulation of the local oscillator. From DC to 10 MHz the substrate noise signal couples resistively into the non-ideal ground lines. The spurs are decreasing with 20 dB/dec with the offset frequency.
- At intermediate frequencies (10 MHz to 100 MHz) the dominant impact mechanism is moving from FM to AM modulation. The amplitude of the spur starts to increase with 20 dB/dec. The main coupling mechanism is the inductor, resulting in AM modulated spurs, which explains the increase of 20 dB/dec.
- At high frequencies, AM modulation is the dominant impact mechanism. The substrate noise impacts increases with 40 dB/dec. The external decoupling capacitors have an effect on the coupling level.
- Close to the LO frequency, injection locking of the VCO occurs. At an offset frequency of 150 MHz from the LO frequency substrate noise starts pulling the LO. When the oscillator is perturbed by a substrate noise signal close to the LO frequency, the LO frequency locks to that of the perturbing signal.

This example shows the great importance the noise frequency has in the coupling mechanisms between the substrate and the oscillator.

A similar example [11] is shown in Fig.2.14 and Fig.2.15. In this case, high frequency noise is

injected in the substrate with a frequency very close to the oscillator fundamental frequency. The perturbed output spectrum shows three components: one is the fundamental VCO output, a second one is at the injected frequency and a third one appears at the opposite side of the VCO output at the same frequency offset as the second one. The author states that this third signal “represents an intermodulation product as a result of the nonlinearity of the VCO” citing Razavi [48] as the reference. Certainly, Razavi blames intermodulation as the cause of the second sideband in [48] but, some years after, the same Razavi publishes a new study [49] analyzing the effect of pulling in unlocked injection locked oscillators where he attributes these sidebands to the frequency modulation of the oscillator caused by the pulling effect.

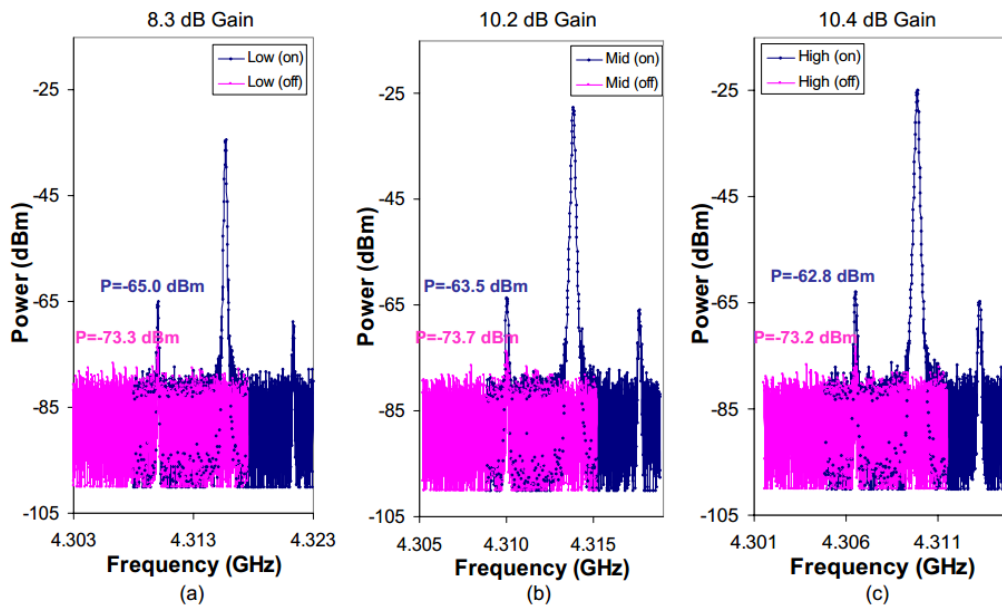


Figure 2.14. 5.2 GHz VCO output with noise on and off for varying biasing current.  $I_{low}=1.81$  mA,  $I_{mid}=2.71$  mA,  $I_{high}=3.41$  mA [11].

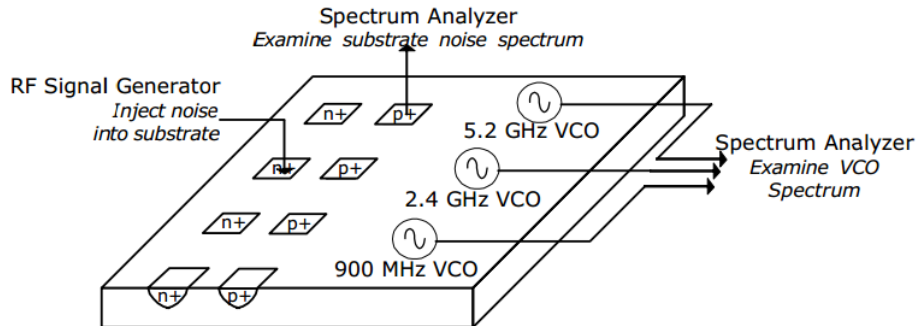


Figure 2.15. Experimental Setup in [11].

In order to investigate a more realistic scenario, a different approach can be taken by placing a real aggressor instead of an injection pad. In an RF transceiver the power amplifier can easily interact with the oscillator due to the high amplitude signals at its output and due to the three different coupling paths between the PA and the VCO: resistive and capacitive coupling through the substrate and magnetic coupling between the PA spiral inductor and the VCO spiral inductor. This situation is shown in Fig.2.16 and Fig.2.17 [50] and has been experimentally reported for example in [51], [52]. It must be noted that in [51] interaction between the VCO and the PA produced inadequate operation of the receiver even if they were placed about 3 mm apart in the same silicon die.

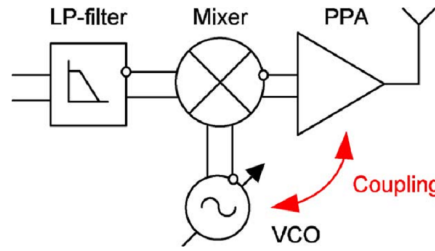


Figure 2.16. Typical transmitter block diagram. The VCO and PA are placed close to each other. [50]

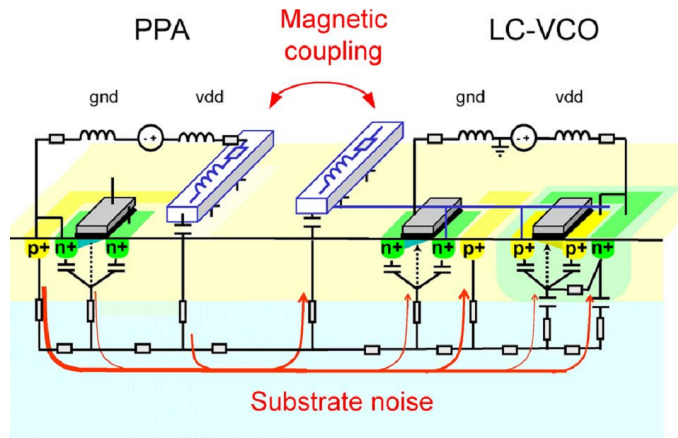


Figure 2.17. Different coupling mechanisms between a PA and an LC-VCO. [50]

The resulting output spectrum of the LC-VCO when the PA is working is shown in Fig.2.18. Several sidebands appear all along the output spectrum showing a relevant interaction between the oscillator and the power amplifier. Authors identify four different different coupling mechanisms:

- electrically through the common substrate;
- magnetically between the on-chip inductors of the PA and LC-VCO;
- magnetically through the bonding wires of both circuits;

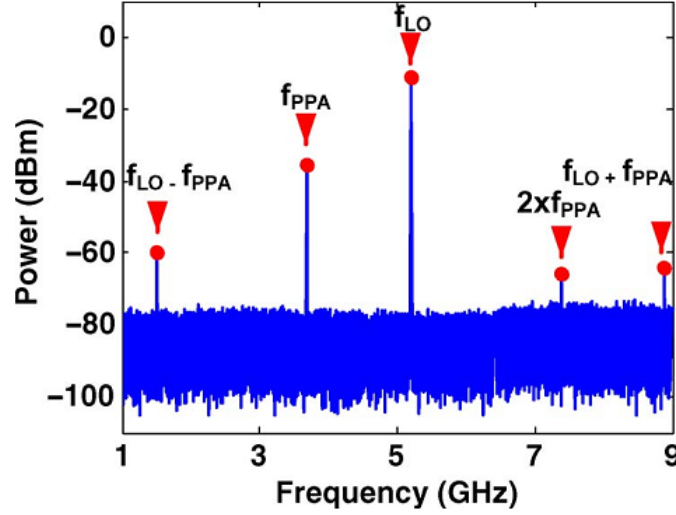


Figure 2.18. Spectrum of the LC-VCO operating at 5.1 GHz when the PA is excited at 3.68 GHz. [50]

- capacitively between the traces of both circuits.

In order to evaluate the level of contribution of the substrate as a coupling mechanism, the die is cut, physically separating the PA from the LC-VCO, as shown in Fig.2.19 left. The results show a big reduction in the LC-VCO performance degradation, like shown in Fig.2.19 right. This experiment shows that, even if the magnetic coupling between the inductors is a relevant source of coupling, the substrate plays a very important role in the LC-VCO degradation.

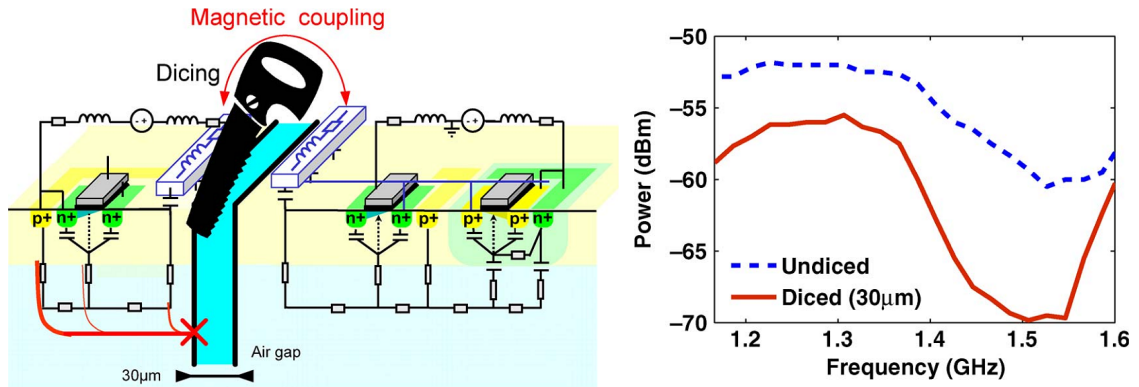


Figure 2.19. Substrate cut test to reduce LC-VCO and PA coupling [50]. Dicing the PA from the VCO test to remove the substrate coupling (left). Measured right-sideband spur( $f_{LO} - f_{PA}$ )of the 5.1 GHz LC-VCO when the PA is excited (right).

Concluding, the high frequency noise traveling through the substrate can harm the performance of the LC-VCO. This effect may affect the design in several aspects: performance degradation, integration limitations, area... The cause of this interaction between noise and the oscillator is not consistently agreed through the literature. Several more contributions are required to increase the

knowledge around this effect. For example, it is necessary to determine the interaction mechanisms between the HFSN and the LC-VCO in order to be able to determine measures to protect the LC-VCO and reduce its performance degradation.

## **2.3 Techniques to mitigate the noise coupling**

Previous section has proven that the noise can travel through the substrate, reach the LC-VCO and degrade its performance. It is extremely important to define measures to reduce this degradation. This section presents the most common measures proposed in the literature.

### **2.3.1 Ground plane optimization strategies**

One of the conclusions obtained by some of the studies in the previous sections is that the non-ideal ground of the VCO is affected by substrate noise currents, that couple, resistively and capacitively, to the ground and flow through its parasitics, causing a voltage bounce. Several authors [12], [46], [53] propose the reduction of the ground plane impedance as the simplest solution to reduce ground bouncing. This solution implies the use of the thickest metal to create a ground plane around the VCO. Implementation of this type of solutions must be made carefully since they are extremely layout-dependent, thus their efficacy should be checked case-by-case. For example, if the mentioned ground plane extends close to a noise-generating circuit, the plane can provide a low-impedance path to the VCO, thus worsening the interaction instead of reducing it. On the other side, minimizing the impedance of the ground plane follows the idea of creating a "good ground", but this does not only depend on the on-chip grounding scheme, but also in the packaging and bonding parasitics, as the same authors recognize in later works [12].

In order to reduce the ground bounce, the noise of the substrate needs to be sunk to a clean ground before it reaches the LC-VCO. P+ type guarding structures are commonly recommended to provide substrate noise currents a return path to ground and keep them out of the VCO circuit ground interconnect. The effectiveness of these guarding structures will be analyzed in the following sections but there is a common characteristic in all of them: the impedance of the return path they provide (ground connections, ground plane) must be very low, at least lower than the impedance to the VCO GND. Usually this requires using a dedicated GND to bias the guard ring structures, with pins separated from those used for grounding the analog circuitry. Fig2.20 shows how a guarding structure

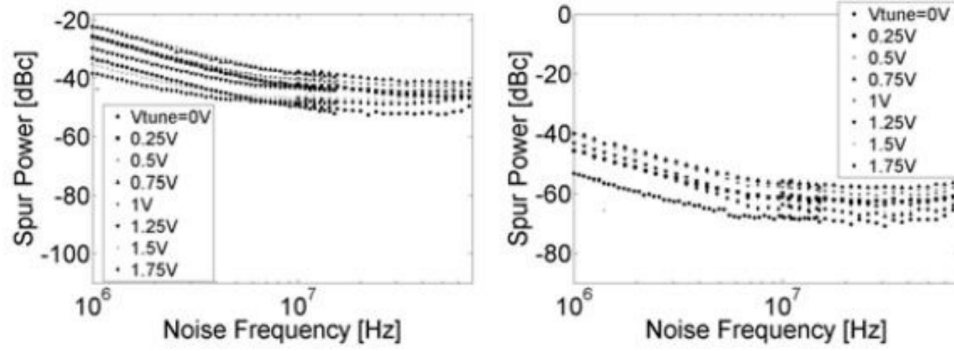


Figure 2.20. Effectiveness of the use of a dedicated bond wire for the substrate guarding structures. No guard ring (left), guard ring with dedicated bonding (right) [54].

connected to the PCB ground using a dedicated bond wires provides around 20 dB of isolation over the solution with a shared bond wire [54].

### 2.3.2 Substrate isolation structures

Once the noise has already reached the substrate, the designer should protect or shield the sensitive parts of the analog systems from the noise generated by the rest of the circuitry, both analog and digital. The basics behind this protection strategies are very intuitive: sink the noise to a clean ground before it reaches the sensitive parts of the circuit. There are several structures available which provide different levels of isolation at different frequencies. These structures can be classified in two main groups:

- Guard rings: A P+ or N+ diffusion surrounding, side by side, the substrate contact to sink the noise to ground.
- Wells: The sensitive element is placed inside of a deep well, completely surrounded by the protection structure.

Finding the optimal structure at the right frequency range with the minimum cost (in area, manufacturing cost or power consumption, for example) is the main challenge for the designer.

The effectiveness of these shielding techniques has been extensively analyzed in the literature from both simulation and empirical point of view. Usually, simulation and real measurement fit very accurately when analyzing test structures with a substrate injection point and a substrate test contact, like shown in Fig.2.22. The test structures can be modeled with a reduced network of resistors and

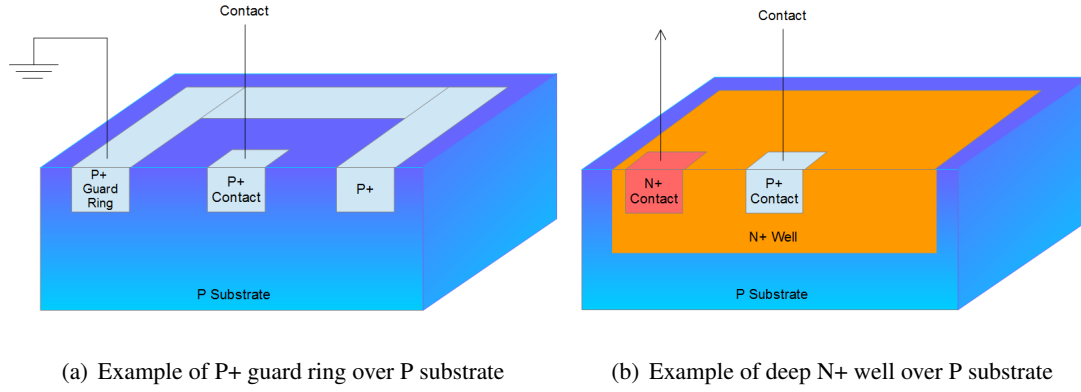


Figure 2.21. Substrate isolation structures

capacitors, like shown in Fig.2.23. Those simplified models allow the simulation of the test structures with very low computational requirements, providing a solid method to evaluate the efficiency of each of the protection structures [55].

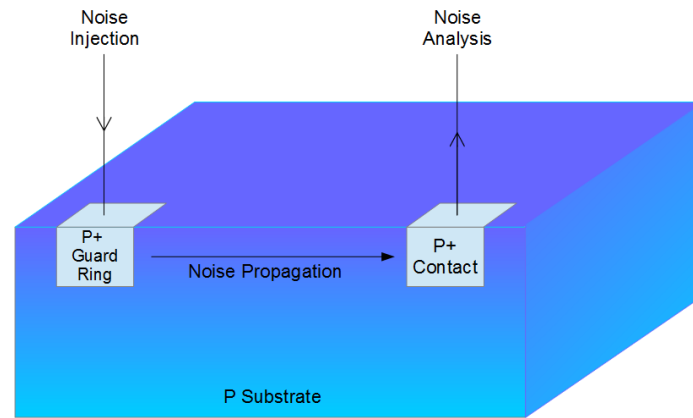
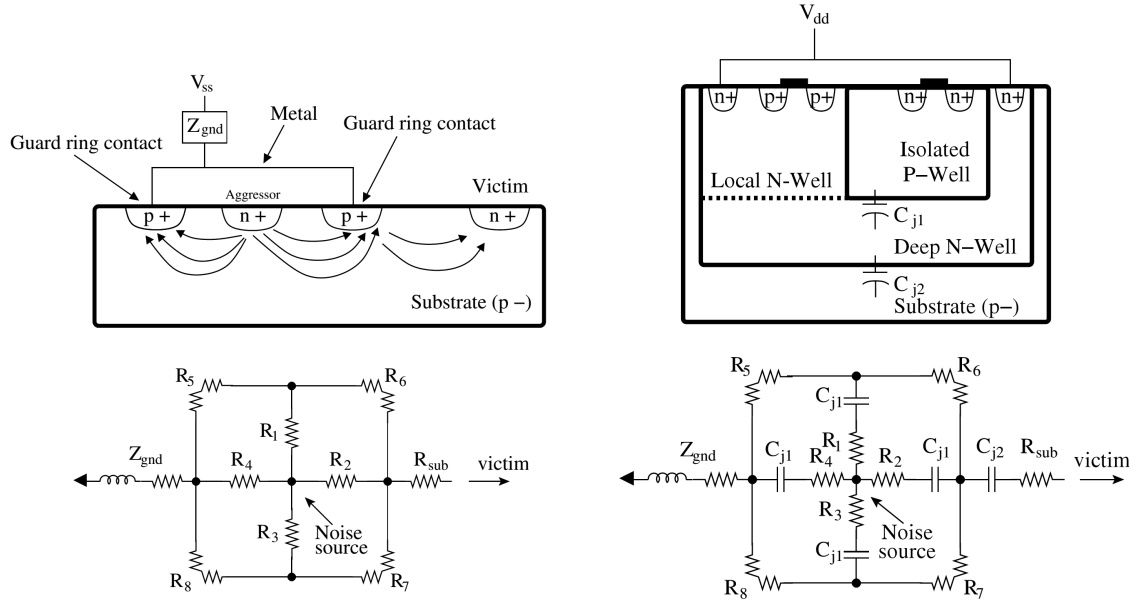


Figure 2.22. Substrate noise test structure

The designer has also available simulation methodologies to co-simulate the effect of guard ring on mixed signal designs [56], [57] together with the 3-D electromagnetic simulators like HFSS [28], momentum [29] or IE3D [30]. The proposed simulation technique of guard ring structures can include all the dependencies with geometric parameters, layout placement and vertical impurities and thus can be strongly helpful to establish isolation strategies against substrate coupling in a given technology. Simulation and measurement results on their investigation (see Fig.2.24) show that the guard ring structures can provide increased isolation of tens of dBs, although with a strong dependency on the frequency and type of structure implemented.

Section 3.2 will deeply analyze and discuss the isolation provided by several different protection structures and their dependance with frequency, but, from the information presented there, one





(a) Guard ring cross-sectional view (top), proposed circuit model (bot). (b) Triple well cross-sectional view (top), proposed circuit model (bot).

Figure 2.23. Substrate isolation structures and their circuit level models [55]

may observe that several authors [56], [58]–[63] have reported very different results for the same structures in very similar technologies, suggesting that the substrate isolation structures can be very effective but the level of efficiency highly depends on other parameters, like for example, the quality of connection to ground or the quality of the ground itself. The main limitation of these structures is that the level of isolation drops as the noise frequency increases. The amount of available information about the efficiency of these structures beyond  $10\text{ GHz}$  is really limited. Anyway, most of these authors agree in the fact that P+ guard rings provide a very effective isolation, especially at low and mid frequencies, at a very reasonable cost (area) without the need to add very costly extra fabrication processes. For this reason, P+ guard rings are commonly used as a low cost solution to improve the substrate isolation.

The geometric characteristics of the protection structures also has an impact on the protection level. An analysis of the level of isolation as a function of the width of the P+ guard ring [47] shows that the isolation of the guard ring against substrate noise does not increase linearly with the width of the P+ layer. The isolation saturates with the width of the P+ layer. Fig. 2.25 shows the proposed structure and test setup as well as the obtained isolation results. The authors also report that the effectiveness of the guard ring also strongly depends on the impedance of the ground connection.

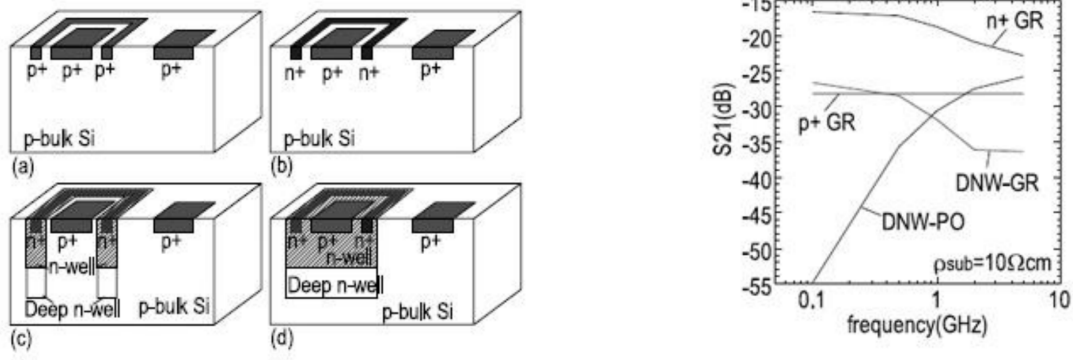


Figure 2.24. Guard ring structures (a) P+ GR (b) N+ GR, (c) deep N -well GR, (d) deep N-well pocket and the simulated S21 versus frequency dependence for these structures [57].

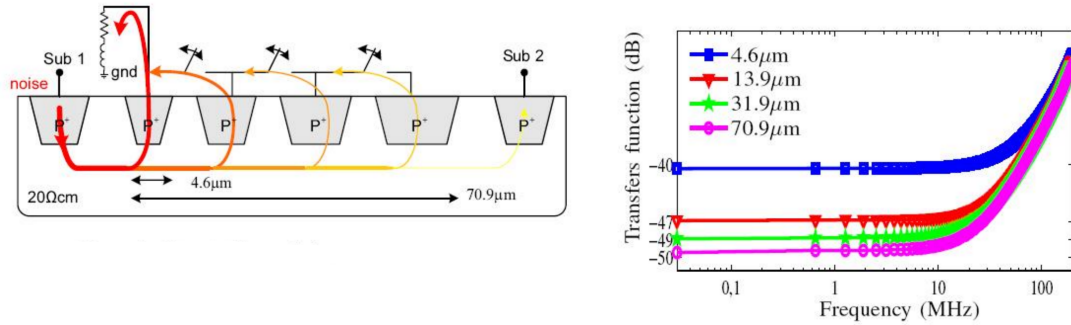


Figure 2.25. Schematic of the sizable guard ring (left) and the transfer functions for different widths of the expandable guard ring (right) [47]

Other authors have also reported the important relationship between the quality of the ground connection and effectiveness of the isolation structures. It is extremely important to minimize the impedance of the current return path. As the frequency increases, the inductance of the return path becomes very relevant [64]. The total impedance is tied to the physical and geometrical characteristics of the layout. This is probably one of the main explanations to justify the high dispersion on the different levels of isolation provided by different authors. An example of the degradation of the isolation level due to the inductance of the isolation structure ground connection is shown in Fig.2.26.

As a conclusion regarding the isolation structures it is possible to affirm that they can provide a substantial level of isolation for some parts of the circuit from the substrate noise but their efficiency depends very strongly on several parameters like geometry, ground connection or noise frequency.

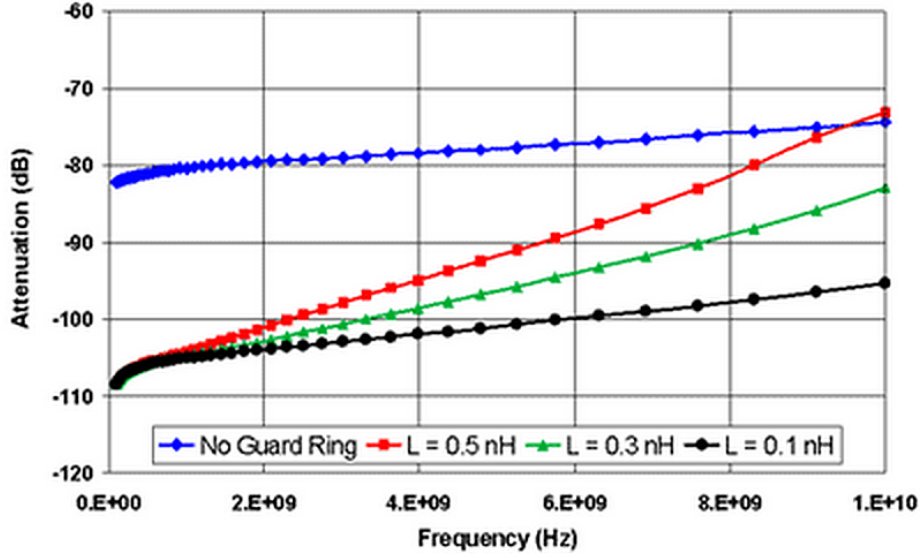


Figure 2.26. Guard-ring isolation as a function of frequency for 0.5, 0.3, and 0.1 nH inductance of the ring ground connection versus no guard ring [64].

### 2.3.3 Inductor shielding

Inductors are usually the largest area components on an RF transceiver. This fact makes them one of the main possible noise paths between the circuit and the substrate because of the large capacitance, both for noise injection and noise picking. On the other hand, currents flowing through inductors create magnetic fields that can penetrate into the substrate, generating noise. Magnetic field can also induce currents on other inductors or interconnects. For all of these reasons, it is very important to take inductors into account when analyzing the coupling mechanisms between RF circuits.

The first documentation about the usage of inductor shielding as a measure to increase the isolation dates from 1998 [65]. In this article the authors present a Patterned Ground Shield (PGS) inserted between an on-chip spiral inductor and silicon substrate. The impact of the shield on inductance, parasitic resistance, capacitance, quality factor and substrate isolation is studied extensively. Results show that the shield increases the inductor quality factor up to 33% and reduces the substrate coupling between two adjacent inductors by as much as 25 dB. Fig.2.27 shows these effects.

There are several different types of PGSs underneath the inductor which may provide different level of improvement on different characteristics of the inductor. Some authors [17] propose that N+ diffusion layer is the most effective layer to place the PGS in terms of quality factor enhancement and substrate coupling reduction between inductors due to the reduced parasitic capacitance, increasing the self oscillation frequency of the inductor. More modern publications [66] support the

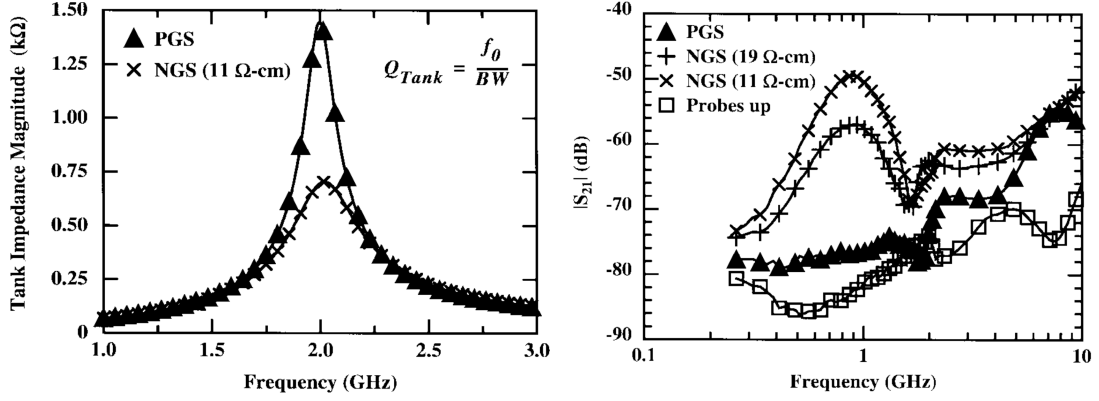


Figure 2.27. Effect of polysilicon PGS on Q of a 2-GHz LC tank (left) and effect of the shield on substrate coupling between two adjacent inductors. [65]

theory about the N+ diffusion layer, designing a double patterned shield using polysilicon and the N+ diffusion layer. Results show some examples where the quality factor of the inductor is increased by 50% reducing the coupled energy to the substrate more than 60%. Other investigations have also confirmed that PGSs on metal layers can provide results as good as n+ diffusion ones [67].

A widely spread investigation line is the discussion about the importance of the shield ground connection. A grounded shield can isolate the inductor from the substrate underneath but can also transmit the ground bounce from the ground network to the inductor. Thus, some authors advocate for floating shields. Moreover, a grounded shield will only be effective if it can sink noise effectively to a clean ground. A test regarding the effectiveness of the ungrounded shield is performed in [68]. Four different test structures are measured to understand the effects on the substrate isolation of each of the inductor grounding methods shown in Fig. 2.28. The comparison of the isolation measurements between the four test cases can be seen in Fig. 2.29. When PGS is well grounded, the substrate noise suppression below 12 GHz is more than 48 dB and is much better than the one when PGS is floating. When PGS is grounded with relevant parasitics, the substrate noise suppression degrades faster at higher frequency. The conclusion of the article proposes that in order to make the design immune to substrate noise, the parasitic inductance and resistance of the on-chip ground connection of PGS have to be kept as low as possible.

It is important to take into account that this result is only valid for single ended (non-differential) inductors. The effectiveness of the floating shield in differential inductors is demonstrated in [69], [70], showing that the floating shield minimizes losses without requiring an explicit on-chip ground connection. Fig. 2.30 shows a symmetric inductor with floating shield. A differential voltage applied

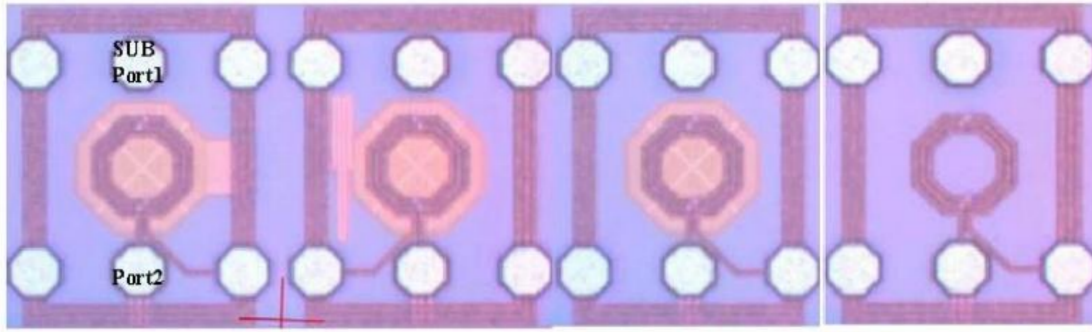


Figure 2.28. Microphotograph of the inductors: (a) PGS is well grounded, (b) PGS is grounded with parasitics, (c) PGS is floating, (d) without PGS [68].

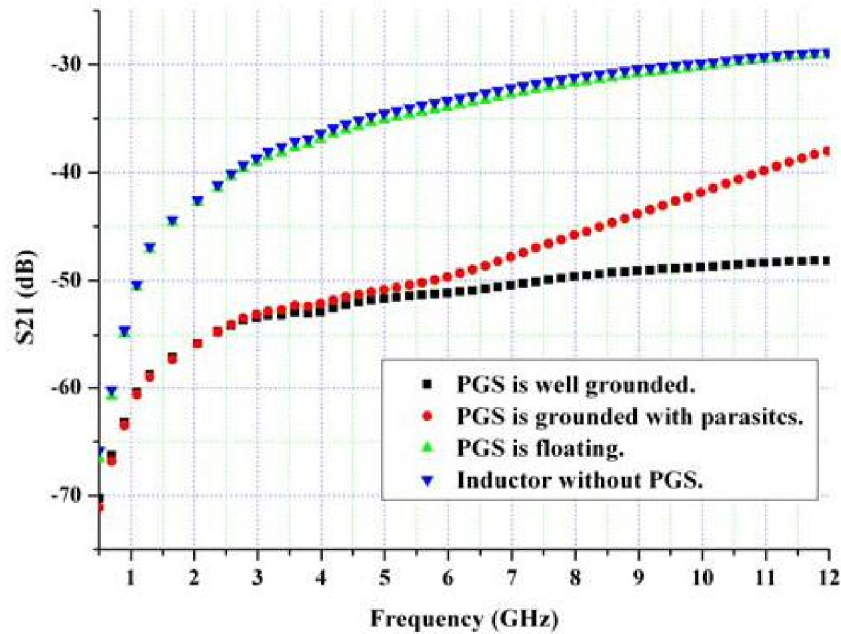


Figure 2.29. Measured isolation between inductor and substrate contact of structures presented in fig. 2.28 [68].

to the inductor winding induces no net voltage onto the shield Metal, blocking capacitive coupled currents from entering the silicon substrate, thereby reducing substrate dissipation and improving the inductor quality factor. The floating shield presents several advantages over the traditional ground shield [69], [70]. First, the floating shield does not need an explicit  $0\text{ V}$  ground reference. Second, the floating shield is not connected to, or directly driven by, AC sources such as transistors. It shields a passive device by electric induction, and can even maintain  $0\text{ V}$  on the shield at mm-wave frequencies due to the virtual ground at the center of the inductor. Moreover, the floating shields of different passive devices are not connected together, so isolation between devices is improved over grounded shields which are connected to a common on-chip ground.

The floating shield technique on differential inductors has been successfully used in the design of

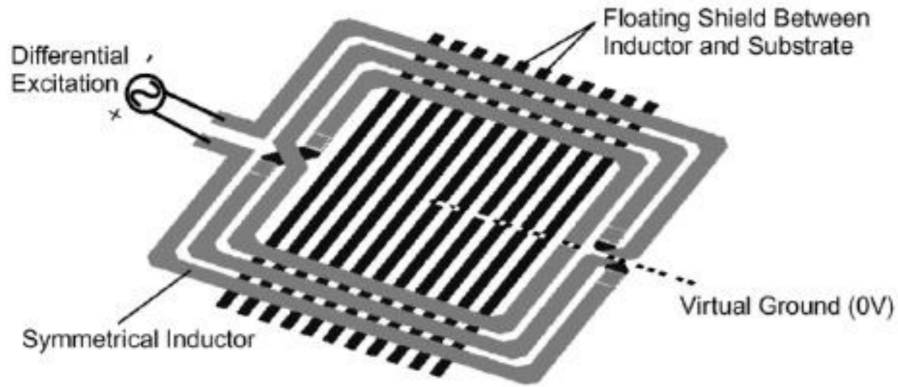


Figure 2.30. Floating ground shield layout showing the virtual ground [69].

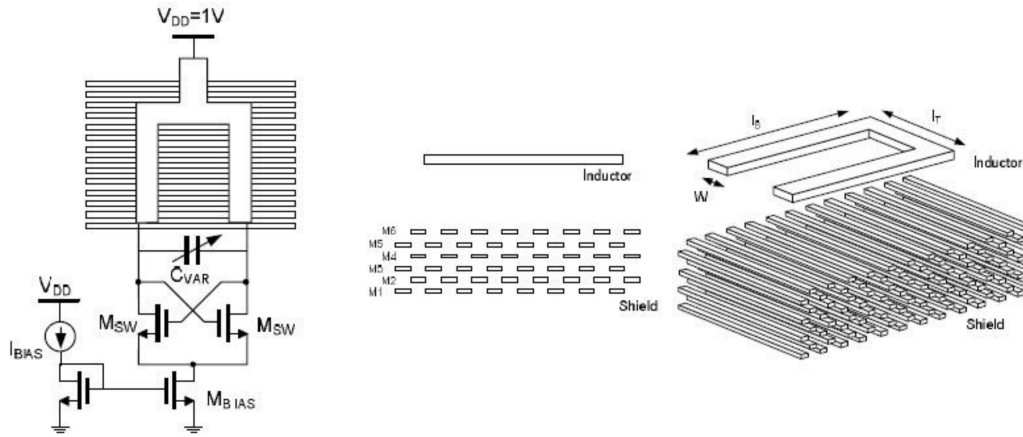


Figure 2.31. Schematic of the 60GHz VCO and floating technique used in the inductor [71].

a 60GHz VCOs [71]–[73]. Fig.2.31 shows the schematic of a VCO and the floating shield technique used for the design of the inductor [71].

The floating shield does not allow the current to flow parallel to the signal path, reducing the loss and increasing the inductance per unit of length [74]. The line is actually behaving as in free space. The strips under the line provide a shield from the substrate. This kind of transmission lines are also known as Slow Wave Transmission Lines [69], [75].

The use of transmission line to replace inductors is common in mm-Wave VCOs. The transmission line provides enough quality factor and can be used to reduce the required design area [75], [76]. The effect of substrate noise on a 60 GHz VCO designed with a transmission line instead of an spiral inductor has also been analyzed [77]. The performance of two VCO designs are compared, one

with an unshielded inductor and one with a Grounded coplanar transmission line. Fig. 2.32 shows a micro-photography of each of the VCOs and the transmission line structure.

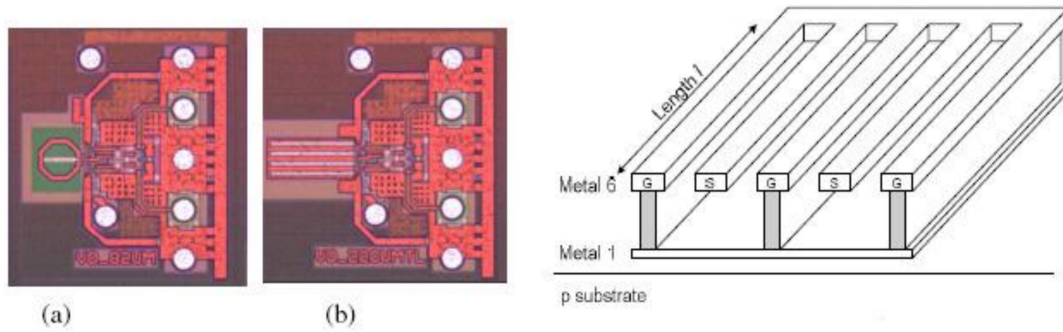


Figure 2.32. Micro-photography of the LC-VCOs with spiral inductor (a) and shorted stub inductor (b) (left). Shorted stub inductor description (right) [77].

The results of the analysis show that although the spiral inductor is favorable in terms of quality factor and self-resonant frequency, the shorted transmission line offers superior isolation from the substrate. The solid ground shield of the transmission line offers reduced sensitivity to substrate interference. The 60 GHz VCO with shorted transmission line as inductor achieves a measured 22.6 dB lower spur power level (see Fig.2.33).

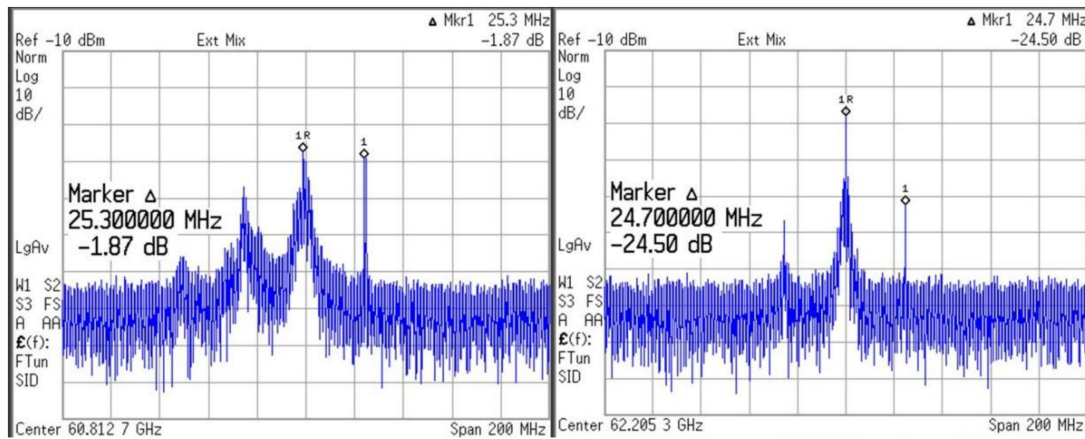


Figure 2.33. VCO output spectrum of the inductor-VCO (left) and the Shorted-stub-VCO (right) [77].

Concluding, the inductor has a very relevant role in the level of robustness of an LC-VCO to substrate noise. A proper design of the inductor can lead to a successful transceiver design but the characteristics or properties that the inductor must have to provide a substrate noise robust LC-VCO are not clearly defined.

## 2.4 Summary and conclusions

The literature presented in this chapter has shown that high frequency noise can easily propagate through the substrate and reach the LC-VCO, degrading its performance. The classical protection structures and noise reduction methods are usually less effective at high frequency. There isn't extensive information about what is the effect of this HFSN on an LC-VCO or what a designer can do to increase the robustness of the oscillator to HFSN. The current state of the art justifies the necessity of a deep analysis of the effect of HFSN on LC-VCOs with the objective to find the interaction mechanisms between the noise and the oscillator. This analysis may lead to find some measures and guidelines to minimize the harmful effects on the oscillator.



## Chapter 3

# Experimental analysis of EM substrate coupling and isolation techniques at RF frequencies.

### 3.1 Introduction

Cost reduction has driven the trend towards the full integration of wireless communication systems in single ICs (RF-SoCs). One of the main design challenges in these SoCs is to isolate the sensitive RF circuits from noise coupled through the substrate, mainly originated by the huge digital processing circuitry. As an example, the total substrate noise produced by an Intel Pentium 4 processor amounts  $190\text{ mV}_{rms}$  ( $1\text{ GHz}$  clock) and around  $7\text{ mV}_{rms}$  if filtered around the  $2.4\text{ GHz}$  or  $5.2\text{ GHz}$  RF bands [78]. These levels are far above the sensitivity levels specified in wireless communications standards, and can also violate requirements regarding the effects of interferers. But besides the noise coupling from the digital section, sensitive blocks can also be affected by couplings from other RF circuits like the power amplifier. Understanding how the noise propagates through the substrate and the selection and implementation of the right isolation techniques on the sensitive circuitry, accounting for the frequency characteristics of each noise source, become then the key factors that allow silicon success. This chapter firstly analyzes the coupling levels between two points of the substrate up to  $40\text{ GHz}$ , with and without isolation structures, with the objective of providing insight about substrate noise propagation and criteria about the efficiency of isolation techniques.

Secondly, this chapter analyzes the role of inductors and substrate in the interaction between analog RF blocks. Isolation between inductors with different geometry and placement is analyzed, as well as the efficacy of techniques to increase this isolation.

## 3.2 Substrate noise coupling and analysis of the efficiency of isolation techniques

This section analyzes the coupling between two contacts on the substrate and the effect that different isolation techniques have on the coupling level. Several works have been published during the last years that evaluate the efficacy of different isolation techniques available in CMOS technology [8], [56], [58]–[63]. Nevertheless, these works often show contradictory results as a consequence of the diverse conditions applied in the reported measurement setups. A broader perspective is needed, where the efficacy of the isolation techniques is compared accounting for measurement and biasing set-up conditions and frequency range of interest.

### 3.2.1 Experiment description

Two different ICs have been manufactured in  $0.35\ \mu m$  and  $0.18\ \mu m$  CMOS processes, containing test structures to experimentally characterize the isolation techniques available in each process. Each test structure consists of two P+ substrate taps separated by a  $50\ \mu m$  or  $100\ \mu m$  distance (pitch), acting as aggressor and victim ports, respectively. The isolation structures are implemented only around the victim port. Each port is connected to larger square pads for on-wafer RF probe access. Two-port S-parameters are measured using a network analyzer, and the effects of probes, pads and interconnect parasitics are de-embedded from the measurements. Fig. 3.1 shows the layout of one of the test structures together with a detail of the aggressor and victim ports. Each port is a P+ diffusion of  $10\ \mu m \times 10\ \mu m$ . P+ guard rings are  $10\ \mu m$  distant from the victim port, and N+ guard rings are  $25\ \mu m$  distant. Two metal lines allow connecting the rings to ground (bottom line) or  $V_{dd}$  (top line). In order to make fair comparisons, these traces are present in all of the test structures, even if they are not needed. The  $V_{dd}$  biasing voltage was introduced through DC probes placed on pads located at the periphery of the die. The substrate of the  $0.35\ \mu m$  technology chip has a nominal resistivity of  $19\ \Omega \cdot cm$ , while that of the  $0.18\ \mu m$  technology is  $10\ \Omega \cdot cm$ . In this second case, a  $1.5\ \mu m$  thick P-well is present, with a resistivity 100 times smaller than the bulk.

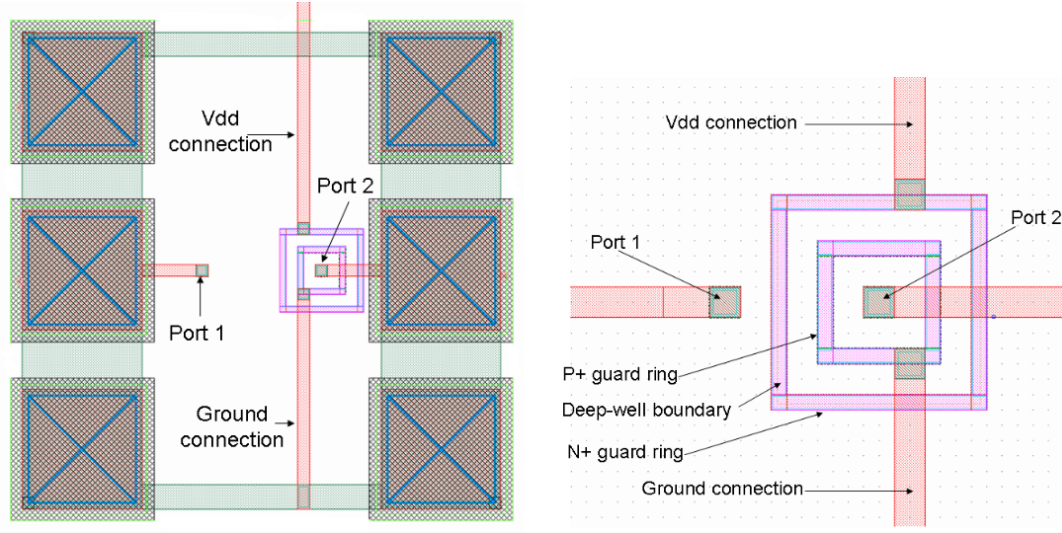


Figure 3.1. Layout of the test structures manufactured.

### 3.2.2 Isolation measurements

#### 3.2.2.1 Effect of distance without isolation

The first set of measurements presented in Fig.3.2 shows the isolation between the ports when no guard ring or triple-well is used. In both cases, increasing the distance from  $50\ \mu m$  to  $100\ \mu m$  provides  $5\ dB$  of increased isolation. Although the geometry of the test structures is the same, the isolation measured for the  $0.18\ \mu m$  technology chip is  $3\ dB$  worse than in the  $0.35\ \mu m$  technology due to its lower bulk resistivity ( $10\ \Omega \cdot cm$  vs.  $19\ \Omega \cdot cm$ ) and the presence of a deep, more conductive P-well in the  $0.18\ \mu m$  technology.  $S_{12}$  is expected to be constant up to some frequency were the dielectric behavior of the substrate becomes relevant and degrades isolation. Often, the limit for dielectric evidence is defined as a cut-off frequency,  $f_c = (2\pi\rho\epsilon)^{-1}$ , where  $\rho$  stands for the substrate resistivity and  $\epsilon$  is its dielectric constant. Nevertheless, this is an arbitrary limit, since the dielectric effect on the value of the substrate impedance is slowly progressive as the frequency increases. For the  $0.35\ \mu m$  process, the former equation says that dielectric effects are expected to appear at  $8\ GHz$ . Estimation of this limit for the  $0.18\ \mu m$  technology substrate is more cumbersome because of the presence of the conductive P-well, but should be  $15\ GHz$  if we account only for the bulk resistivity value. The plots in Fig.3.2 confirm these estimations. The abrupt isolation degradation observed above  $10\ GHz$  and the fact that the curves for the  $50\ \mu m$  and  $100\ \mu m$  distances tend to match, suggest an important contribution of the direct coupling between pads.

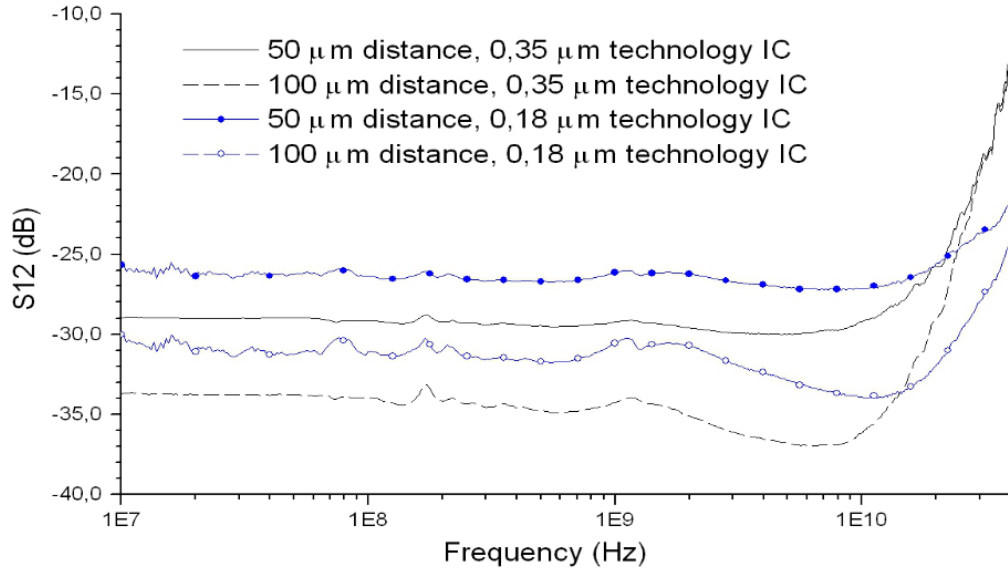


Figure 3.2. Default substrate isolation between aggressor and victim (no guard ring nor triple-well applied).

### 3.2.2.2 Effect of guard rings

Concerning the isolation added by guard rings enclosing the victim port, three cases are considered: a single grounded P+ ring; a single N+ ring connected to  $V_{dd}$ ; and both P+ and N+ rings (only in the  $0.18 \mu m$  process). The results obtained for a  $50 \mu m$  distance between ports are shown in Fig. 3.3. Results for a  $100 \mu m$  distance were also obtained for the  $0.18 \mu m$  process chip, with no relevant qualitative differences. The larger isolation is provided by the grounded P+ ring, which increases by  $30 dB$  the isolation at low frequencies, independently of the distance between ports or the technology node. Beyond  $1 GHz$ , this isolation is progressively lost, initially at a  $10 dB/dec$  rate and later more abruptly. Substrate and parasitic extraction with Assura software shows that this degradation of the P+ ring efficacy is due to the increasing impedance offered by the GND connection, due to inductive effects. This phenomena has also been reported in [62] and [79]. The isolation offered by the N+ guard ring is different in both technologies because of the different characteristics of the ring: a shallow diffusion in the  $0.35 \mu m$  process, which results in no added isolation at low frequencies; an N-well in the  $0.18 \mu m$  process, which results in approximately  $5 dB$  of isolation enhancement. This result suggests that a significant amount of noise flows along the conductive P-well, which is approximately the same depth as the N-well ring. Note that, because of the high-impedance connection of the N+ rings to  $V_{dd}$ , they don't serve as return paths for the noise, but only as "current blockers". This is further discussed in the following section.

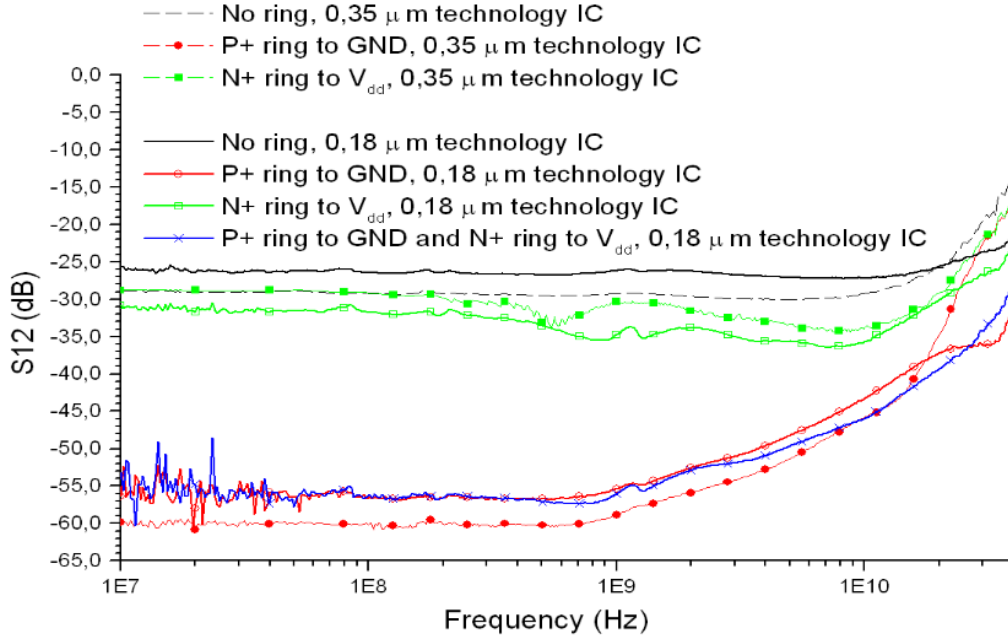


Figure 3.3. Measured isolation provided by guard rings of different types, for a  $50\text{ }\mu\text{m}$  distance between ports.

### 3.2.2.3 Effect of triple wells

Triple wells were only supported by the  $0.18\text{ }\mu\text{m}$  process, therefore, measurements are presented only on this process. Fig. 3.4 shows the results obtained, for the triple-well alone and for the triple-well plus a grounded P+ ring. Results are not very accurate in the  $10\text{-}100\text{ MHz}$  range because of the low signal levels measured; therefore we will focus our discussion above  $100\text{ MHz}$ . Measurements in Fig. 3.4 show that isolation provided by the capacitance of the reversed biased junction diodes is degraded as frequency increases, although some resonances due to the complex  $V_{dd}$  interconnections produce non-monotonous behavior. The isolation of the triple-well is excellent at low frequencies, but the junction capacitances already behave like a short at frequencies in the  $10\text{ GHz}$  range, and the beneficial effect of the triple-well is lost. Note that, since in this case the isolation is basically provided by the junction, no significant dependence on the distance between ports is observed. A guard ring inside a triple-well adds about  $20\text{ dB}$  of isolation respect to the triple-well alone. Compared to a grounded P+ guard ring alone (Fig. 3.3), a triple well looks a worse option for the frequency under measurement, but if we extrapolate the average slope observed in the  $100\text{ MHz-}1\text{ GHz}$  range to lower frequencies, then it is evident that the triple well will result more advantageous for frequencies low enough. Moreover, a good  $V_{dd}$  biasing can drastically improve isolation, as discussed in the next section.

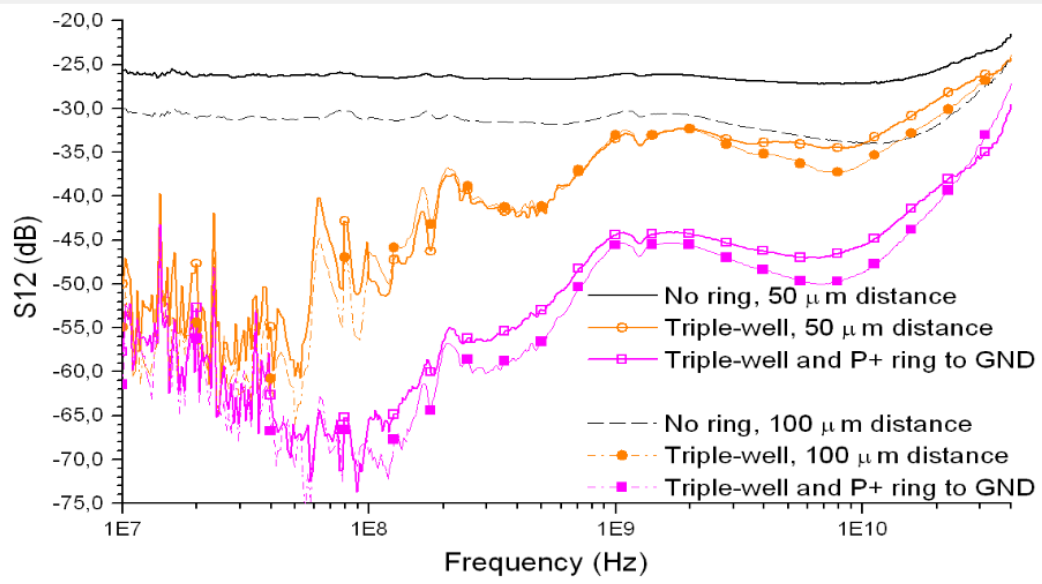


Figure 3.4. Measured isolation provided by a triple-well.

### 3.2.3 Discussion and design recommendations

#### 3.2.3.1 Comparative analysis

Table 3.1 compares  $S_{12}(\text{dB})$  at  $50 \mu\text{m}$  and  $100 \mu\text{m}$  distance (pitch) for our two test circuits, against those reported in previous experimental works. The isolation values present variations associated to the technology characteristics or contact size. It is remarkable to note in [56] that the isolation is significantly worsened with increased contact size, thus a significant dependence is to be expected with the area of the victim device (eg., a single transistor, an spiral inductor or an array of grounded taps will show decreasing isolation for the same distance to a given noise source).

Source	$S_{12}$ @ distance 1	$S_{12}$ @ distance 2	Ports size
This work	-29 dB @ $50 \mu\text{m}$	-34 dB @ $100 \mu\text{m}$	$10 \mu\text{m} \times 10 \mu\text{m}$
This work	-26 dB @ $50 \mu\text{m}$	-31 dB @ $100 \mu\text{m}$	$10 \mu\text{m} \times 10 \mu\text{m}$
[58]	-28 dB @ $50 \mu\text{m}$	-38 dB @ $100 \mu\text{m}$	$10 \mu\text{m} \times 10 \mu\text{m}$
[56]	-12 dB @ $50 \mu\text{m}$	-19 dB @ $100 \mu\text{m}$	$50 \mu\text{m} \times 50 \mu\text{m}$
[62]		-29 dB @ $145 \mu\text{m}$	$25 \mu\text{m} \times 25 \mu\text{m}$

Table 3.1. Reported isolation values between two ports.

We compare now in Table 3.2 the added isolation provided by a grounded P+ ring against that reported in other experimental works. Comparison is made in all cases for a frequency around  $1 \text{ GHz}$ .

The disperse results in Table 3.2 indicate that the effective isolation that can be achieved with a guard ring depends strongly on implementation details (presence of a conductive P-well, ring distance and width, etc). In all cases the P+ guard ring is a very good option, but the added reported isolation varies from 10 *dB* to 40 *dB* depending on the work. In all the cases, the isolation increase remains independent of frequency up to 1 *GHz*, but as it is shown in section II, a degradation of the guard ring efficacy appears for frequencies in the *GHz* range because of inductive effects in the GND node. It must be noted that, in all the works reported in Table 3.2, RF probes were used for grounding and the test structures were only a few hundred microns wide, therefore the series inductance of the ground connection was always very small. In real SoCs, package effects and large GND distribution networks would degrade the isolation offered by guard rings already at frequencies well below 1 *GHz*.

Author	Isolation increase when adding P+ to GND
This work	+30 <i>dB</i>
[58]	+15 <i>dB</i>
[56]	+10 <i>dB</i>
[59]	+15 <i>dB</i>
[60]	+15 - 20 <i>dB</i>
[61]	+30 - 40 <i>dB</i>
[62]	+36 <i>dB</i>
[63]	+10 <i>dB</i>
[80]	+18 <i>dB</i>

Table 3.2. Reported isolation added by P+ grounded guard rings around the victim port.

Last, Table 3.3 lists the reported isolation added by triple-well structures enclosing the victim port. Again, the reported isolation values depend strongly on the implementation of the well and technology characteristics. In this case, there is an extra variable, which is the impedance of the  $V_{dd}$  connection used to bias the N-well. We can distinguish two effects that contribute to add isolation in a triple-well structure: one, the capacitance of the PN junctions that are found in series in the propagation path, and two, the AC return path provided by the  $V_{dd}$  biasing of the N-well. The isolation added by the first effect is excellent near DC, but is progressively lost with increasing frequency, up to where the PN junction presents negligible impedance. On the contrary, the effect

as a return path will show excellent isolation up to higher frequencies. In our experimental setup, the  $V_{dd}$  connection offered high impedance, therefore only the contribution of the series capacitance remained, resulting in measured isolation values worse than a P+ ring. In other cases (clearly the case of [58] and [62]), a frequency dependence is observed at low frequencies but later isolation saturates to extremely good values, even better than those offered by P+ rings. The reason for this is that the conductivity of N-well/N+ regions is better than that of P-well/P+ ones. Thus, such techniques based on offering extra return paths to AC ground are better when implemented in N than when implemented in P-type regions. This is the case of [62], where simple N+ rings offer better isolation than P+ rings.

Author	Measured @ 500 MHz	Measured @ 5 GHz
This work	$\sim +15\text{ dB}$	$\sim +5\text{ dB}$
[58]	$+50\text{ dB}$	$\sim +30\text{ dB}$
[56]	$\sim +30\text{ dB}$	$\sim +10\text{ dB}$
[59]	$\sim +40\text{ dB}$	$\sim +20\text{ dB}$
[62]	$\sim +70\text{ dB}$	$\sim +50\text{ dB}$
[8]	$\sim +8\text{ dB}$	$\sim +0\text{ dB}$

Table 3.3. Reported isolation added by a triple well isolating the victim port.

### 3.3 Modeling and experimental characterization of EM coupling between integrated spiral inductors

Spiral inductors are essential elements in the design of RF transceivers. The performance of most of their circuits depends closely on the parameters of the inductors, namely their inductance and quality factor at the frequency of interest, and in consequence a lot of effort has been devoted in the last years to their optimization and accurate modeling. Nevertheless, the inductors are modeled as if they were independent elements, when in fact magnetic field lines close between neighbor inductors, giving rise to a mutual inductance. Also, mutual capacitance and substrate can be other means of coupling. While some CAD tools already incorporate substrate extractors to take into account substrate coupling between devices [81], mutual inductance and capacitance are typically ignored, neglecting a significant effect for near components. It must be noted that edge to edge



distance between inductors in the same circuit (ex., LNA) can be less than  $100\ \mu m$ , while distances in the range of  $200\text{-}300\ \mu m$  can be considered typical between inductors of different circuits. The effect of mutual coupling on these circuits may show in different ways. On the one hand, mutual inductive coupling modifies the effective self-inductance value of the component, which may provoke a bad tuning of the design, particularly in resonant circuits. On the other hand, mutual coupling may induce undesired interaction between signals, in the form of noise injection or crosstalk. Previous works have shown examples of circuits where the effect of mutual coupling between inductors shows to be relevant. In [82], an LNA is presented where mutual coupling between inductors produces a decrease of  $4\ dB$  for the gain at the desired frequency. Another LNA circuit is presented in [83], where coupling between inductors in the LNA and buffer degrade the reverse isolation by  $10\ dB$  at the frequency of interest. Last, a free-running resonant VCO is shown in [82] that becomes injection-locked to another near VCO for small frequency offsets.

Commonly, substrate is the only means of coupling between RFIC devices that is taken into account during the design phase. In the case of inductors, EM coupling is added to the substrate coupling, but it is often neglected during the design, particularly for circuits operating in the low-GHz range. In this section, we present a detailed study of the behavior of mutual inductive coupling, supported by experimental results, that extends the frequency range analyzed in previous works [84], [85], and we introduce a new model valid up to the inductors resonant frequency. The typical coupling behavior up to frequencies beyond the inductors resonant frequency is presented, the observed behavior is explained and an electrical model validated against EM simulations is proposed and validated. A complete study of coupling dependence on different geometrical parameters is also presented in this section and valuable design recommendations are proposed. Finally, experimental measurement results are presented, which validate the EM simulations and the previously performed analysis.

### 3.3.1 Experiment description

Fig. 3.5 shows the typical situation analyzed in this section, where two identical inductors are placed nearby thus they exhibit a significant coupling. Both of the inductors have one of their ends grounded, while the other end is connected to a  $50\ \Omega$  terminated port. An S-parameter measurement allows obtaining the mutual coupling, as well as other parameters of interest (self and mutual inductance, self-resonant frequency).

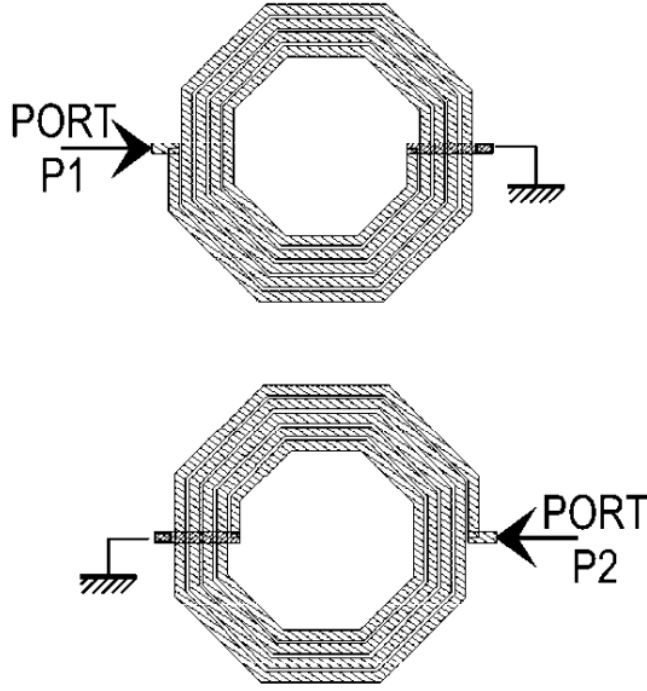


Figure 3.5. Scheme of two coupled inductors analyzed in this work.

The layout in Fig.3.5 is simulated with Agilent Momentum [29], with parameters corresponding to a  $0.35\ \mu m$  technology. Inductors are laid in the top thick metal-4, while the reference terminal is placed in the backside plane of the substrate with resistivity  $20\ \Omega \cdot cm$ . Fig.3.6 shows the coupling measured in the simulations, for a center to center inductor distance of  $225\ \mu m$ . It can be observed that below the RF domain, coupling increases with frequency at a rate of  $20\ dB/dec$ . At a certain frequency  $f_p$ , the trend changes and coupling starts to decrease with increasing frequencies, while a second trend change is observed at a frequency  $f_z$ , above which coupling increases again. This behavior can be considered typical as far as manifests in all the situations analyzed in this work, including measurements, and to the best of our knowledge, at the moment of the original publication, it was the first time that the behavior at high frequencies was described.

### 3.3.1.1 Inductor coupling modeling

The behavior observed in Fig.3.6 can be understood from an electrical model of the situation. We will first concentrate in the first half of the curve, i.e. up to the negative slope. Fig.3.6 shows a lumped model of the two coupled inductors, obtained from a classical model of two simple inductors [86], where magnetic, capacitive and substrate conductive coupling have been added.

In this model,  $L_i$ ,  $R_{Li}$  and  $C_{Li}$  stand for each inductor self-inductance, series resistance and

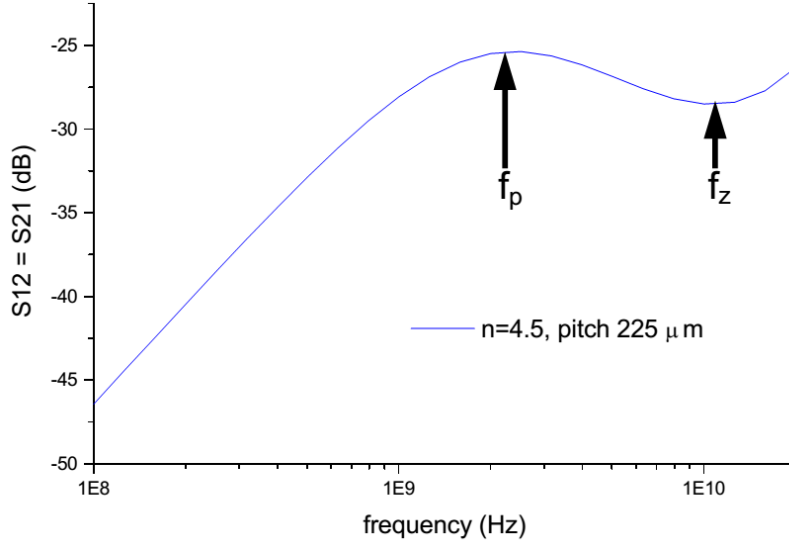


Figure 3.6. Coupling obtained from Momentum simulation of two coupled inductors, pitch  $225 \mu m$ .

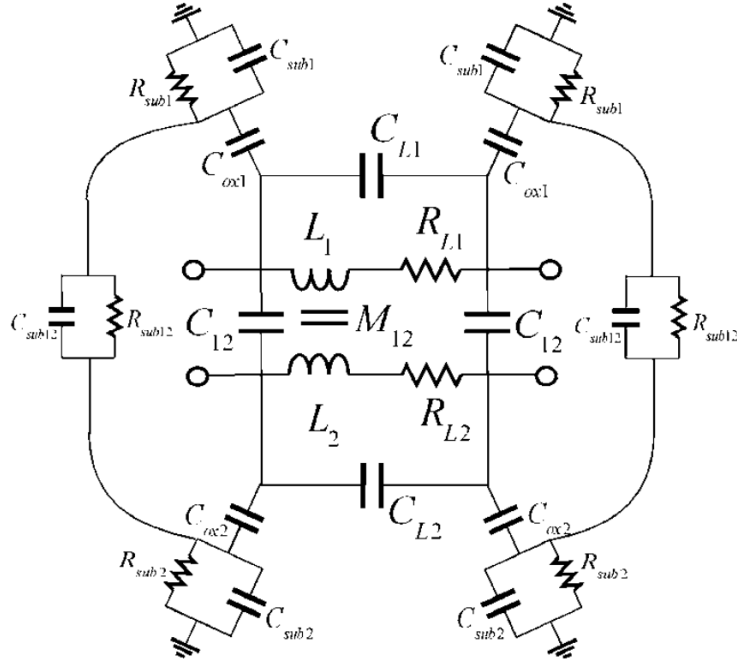


Figure 3.7. Lumped electrical model of two coupled inductors.

self-capacitance, respectively.  $C_{oxi}$  is the oxide capacitance to the substrate, while  $R_{subi}$  and  $C_{subi}$  model the substrate parasitics between the inductors and the reference terminal. All these values can be estimated from technology and geometric characteristics, as described in [87]. Coupling between inductors is modeled with  $M_{12}$  and  $C_{12}$ , which stand for the mutual inductance and capacitance through the dielectric, while  $R_{sub12}$  and  $C_{sub12}$  model the coupling through the substrate. If the frequency range of interest is limited to a few GHz, this complete model can be simplified by

neglecting substrate capacitance  $C_{sub}$  and self-capacitance  $C_L$ . Other elements, such as  $R_L$ ,  $R_{sub}$  or  $C_{12}$ , can also be of minor importance for the coupling estimation, depending on geometrical or technology characteristics. Stripped to its essentials, the model is reduced to its inductive elements. After grounding one of the ends of each inductor, while connecting the other end to a resistively terminated port, and transforming the model to its T equivalent, we obtain the simplified circuit of Fig. 3.8, which is essentially the basic model of a transformer [86].

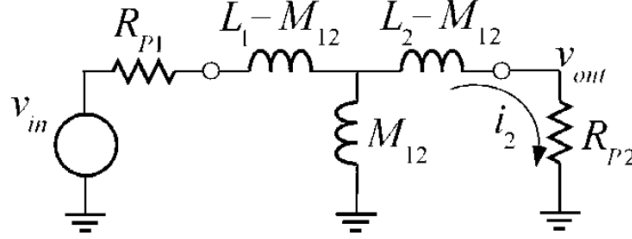


Figure 3.8. Simplified electrical model of two coupled inductors terminated with resistive ports.

A simple circuit analysis of this simplified model leads the following expression for the voltage gain:

$$\frac{V_{out}}{V_{in}} = R_{p2} \frac{sM}{(L_1 L_2 - M^2) \left( s + \frac{R_{p1} L_2}{L_1 L_2 - M^2} \right) \left( s + \frac{R_{p2} L_1}{L_1 L_2 - M^2} \right)} \quad (3.1)$$

According to this expression, coupling presents a zero at the origin, which explains the initial  $20 \text{ dB/dec}$  slope in Fig. 3.6, and two poles that provoke a slope change at some frequency. For the particular symmetric situation analyzed in Fig. 3.6, where  $L_1 = L_2$ , and  $R_{p1} = R_{p2}$ , the gain can be reduced to expression (3.1), and the poles are located at the same frequency  $f_p = \frac{R_p}{2\pi L}$ . An inductance value of  $L = 4.07 \text{ nH}$  was obtained from simulations of the inductors in Fig. 3.5, therefore a frequency  $f_p = 1.95 \text{ GHz}$  is predicted for the poles location, which matches the results shown in Fig. 3.6.

$$\frac{V_{out}}{V_{in}} = R_p \frac{sM}{(L^2 - M^2) \left( s + \frac{R_p L}{L^2 - M^2} \right)^2} \approx R_p \frac{sM}{L^2} \frac{1}{\left( s + \frac{R_p}{L} \right)^2} \quad (3.2)$$

According to this expression, it is expected that for frequencies below the poles at  $f_p$ , coupling will be independent of  $L$ , and depend linearly with the mutual coupling  $M$ . On the contrary, for frequencies above  $f_p$ , it is expected that coupling will depend on  $M/L^2$ .

Fig. 3.9 compares the voltage gain obtained from expression (3.2), against the complete model in Fig. 3.7, and the EM Momentum simulation of the inductors in Fig. 3.5. It can be verified that

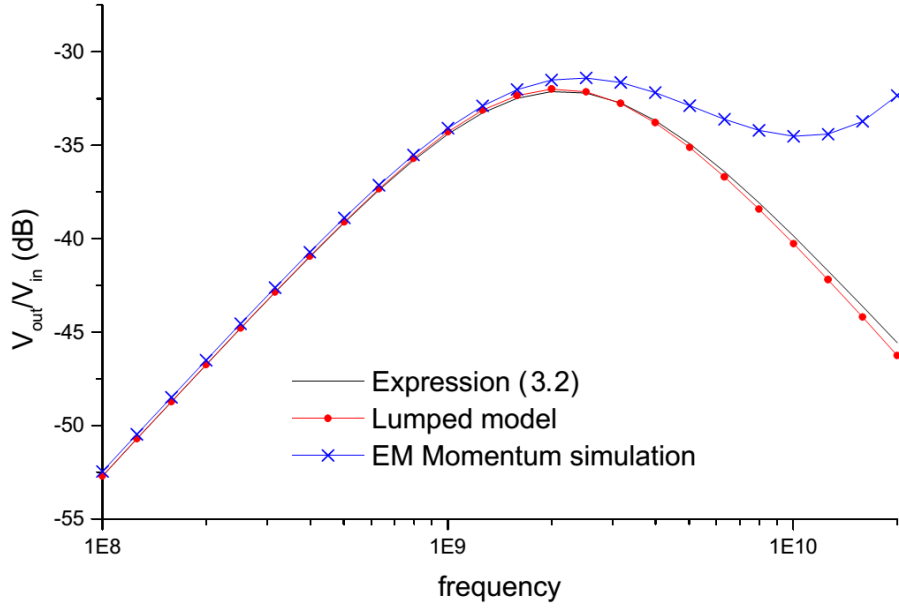


Figure 3.9. Coupling as predicted by expression (3.2), compared against complete lumped model and EM Momentum simulations.

the simplified model matches perfectly the coupling behavior up to the first slope change at  $f_p$ , while neither the simplified nor the complete lumped model are able to accurately predict the second slope change that appears at  $f_z$ . It can be seen that, although accurate modeling above  $10\text{ GHz}$  may have a limited interest (the resonant frequency of the inductors is near  $10\text{ GHz}$ ), modeling the second slope change is necessary to accurately predict the coupling in the frequency range between  $f_p$  and  $f_z$ . We have verified that frequency-dependency of the model elements in Fig. 3.7 is not the responsible for the mismatch at high frequencies of the curves in Fig. 3.9. On contrary, we have identified the unsymmetrical, lumped nature of the model in Fig. 3.7 as responsible for the high frequency mismatch. A simple transformation of the lumped model into a distributed model, proportionally scaling the values according to their series or parallel placement, leads to an accurate prediction of the second slope change in the coupling. Fig. 3.10 plots the simulation of a 5-stage distributed version of the model in Fig. 3.7, against the EM Momentum simulation. It can be checked that now the model correctly predicts  $f_z$  and the coupling increase above  $10\text{ GHz}$ . A maximum mismatch of  $1\text{ dB}$  is appreciated at  $8\text{ GHz}$ , which is considered a tolerable error. It is well known that at that frequency range some parameters exhibit significant frequency dependency, which is probably responsible for the small mismatch between the model and the simulations.

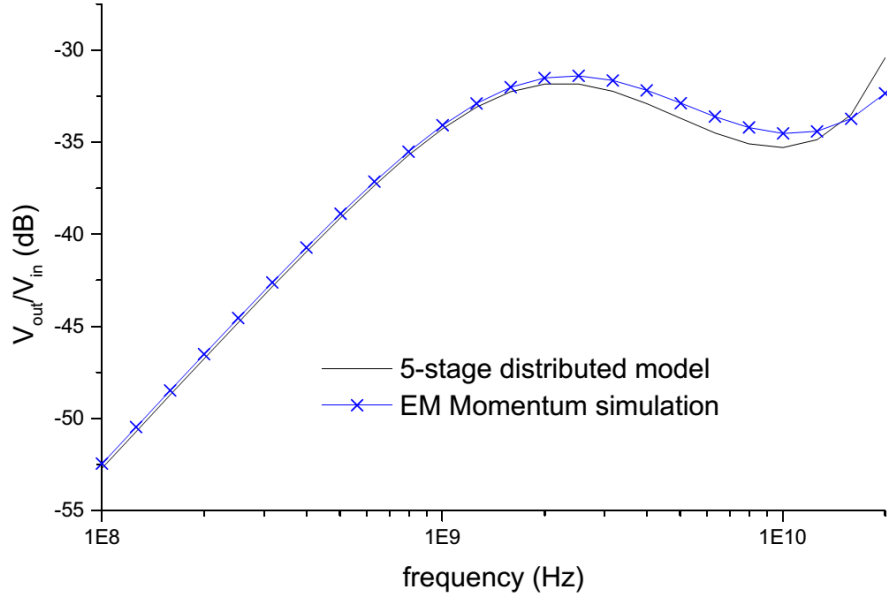


Figure 3.10. Coupling as predicted by a 5-stage distributed version of the model in Fig. 3.7, compared against an EM Momentum simulation.

### 3.3.2 Coupling dependence with geometry.

Starting from the reference layout shown in Fig. 3.5, a set of EM Momentum simulations has been performed changing different geometry parameters, including those parameters of the inductors. This will allow validating the conclusions obtained in the previous section, as well as understanding which parameters contribute to increase coupling. Fig. 3.11 shows the mutual coupling obtained when the number of turns of the inductance increases, while maintaining the inner radius. The figure includes the self and mutual inductance, at low frequencies, obtained from simulation. As expected, both self and mutual inductance increase with the number of turns. The coupling level at low frequencies increases with  $M$ , as predicted by equation (3.2), while the increasing values of  $f_p$  respond to decreasing  $L$ , and it can be checked that their values match those predicted by the model. Above  $f_p$ , the effect of  $L$  compensates the increase of  $M$ , also as predicted by equation (3.2).

Fig. 3.12 also shows the coupling dependence on the number of turns of the inductors, but now maintaining constant the external radius. The contribution of the inner turns to the self-inductance  $L$  is smaller than those of the external turns, but it is remarkable that the contribution of these inner turns to the coupling inductance  $M$  is even smaller than to the self-inductance. As a consequence, coupling at low frequencies exhibits now a modest dependence with the number of turns. The frequency  $f_p$ , which depends on  $L$ , exhibits the expected behavior, as well as the coupling above  $f_p$ , which now is higher for smaller number of turns due to their smaller inductance  $L$ .

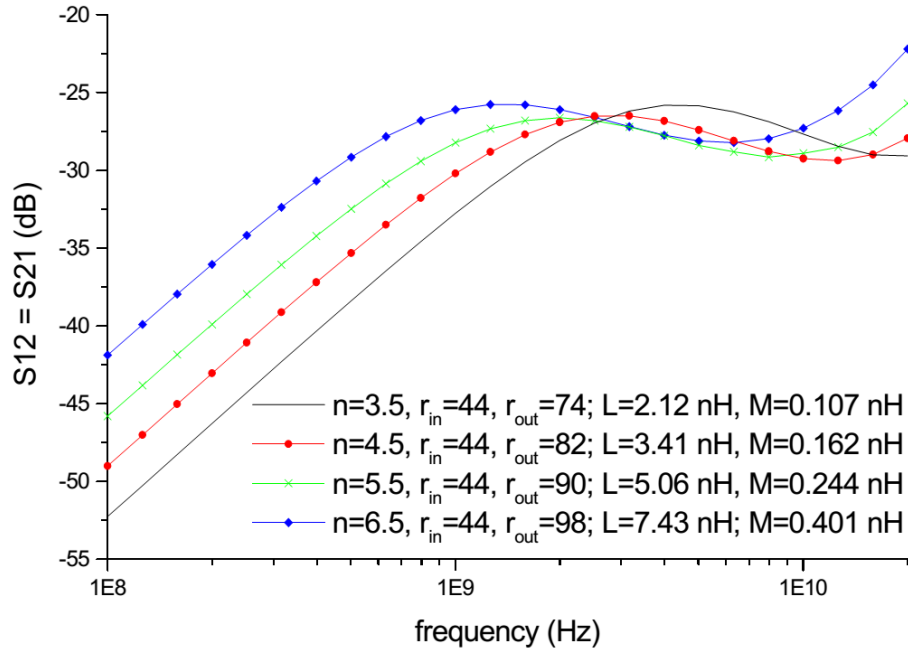


Figure 3.11. Dependence of the mutual coupling on an increasing number of external turns of the inductors.

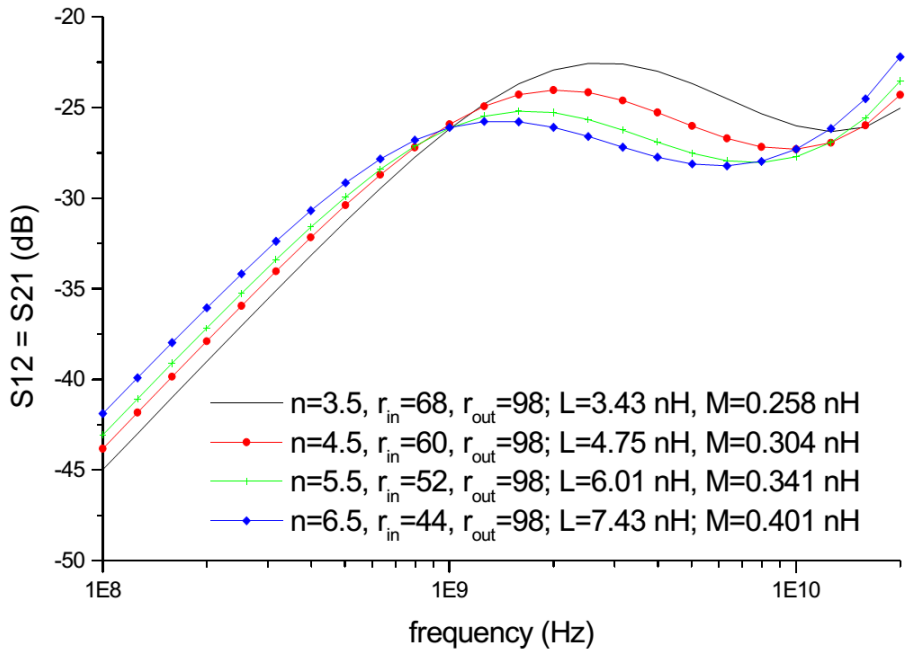


Figure 3.12. Dependence of the mutual coupling on an increasing number of internal turns of the inductors.

Coupled inductors of 3.5 turns, but with increasing internal (and external) radii have been also simulated and results shown in Fig. 3.13. As expected, higher radius produce higher inductance  $L$ , but again it is remarkable the strong dependency of  $M$  with this parameter. It must be noted that inductor pitch was kept constant in these simulations, thus a larger spire radius means closer distances

between inductor edges. This combined dependence of both the distance and the total magnetic field on the radius explains the dependencies of  $M$  observed in Figs. 3.11, 3.12 and 3.13.

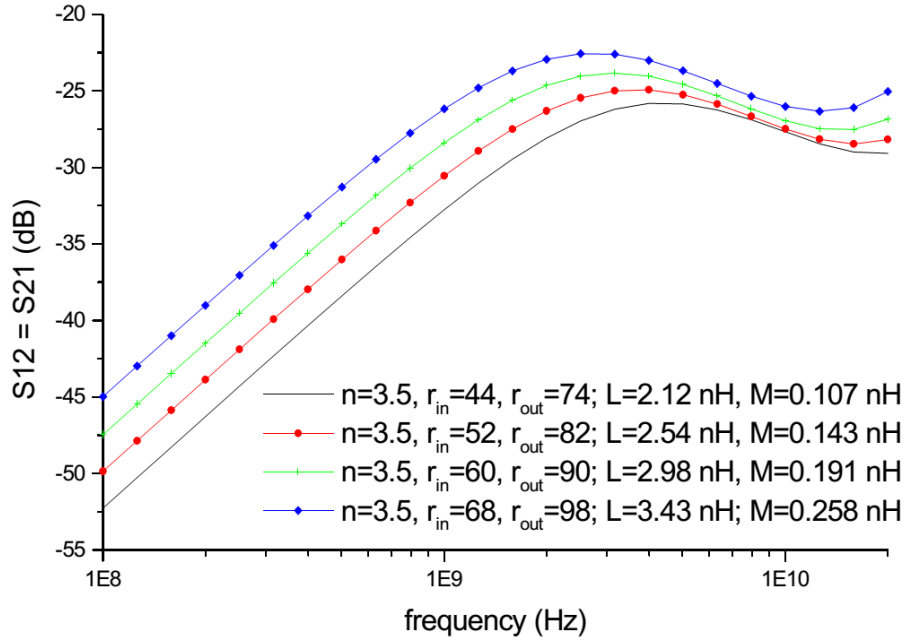


Figure 3.13. Dependence of the mutual coupling on the inductors radii, while maintaining constant the number of turns.

The dependence with distance between inductors is now explored, and the results are shown in Fig. 3.14. Here, the inductors have always 6.5 turns, but the pitch (center to center distance) is increased. As expected, the magnetic coupling  $M$  decreases with increasing distances, while the inductance  $L$ , which depends on the unchanged inductor parameters, remains constant. According to the model, the frequency  $f_p$  will remain constant for the different distances, while coupling will exhibit the same dependence with  $M$  both below and above  $f_p$ . This is exactly the same behavior observed in the EM simulations results plotted in Fig. 3.14.

Fig. 3.15 shows now the results obtained for the 4.5 turns inductor, in function of the ratio  $w/s$ , where  $w$  stands for the width of the inductor spires, and  $s$  for their separation. Since the addition  $w+s$  remains a constant value, the internal and external radii of the inductors remain constant,  $r_{in} = 44 \mu m$  and  $r_{out} = 98 \mu m$ . In consequence, the inductance  $L$  and  $M$  will show negligible variation, as seen in Fig. 3.15. On the contrary, the spire width has a strong impact on the inductor quality factor, as observed in the values included in Fig. 3.15, since narrower lines will produce higher losses. Therefore, increasing the ratio  $w/s$  provides a way to increase the quality factor of the inductors without modifying neither their self-inductance nor their mutual coupling.



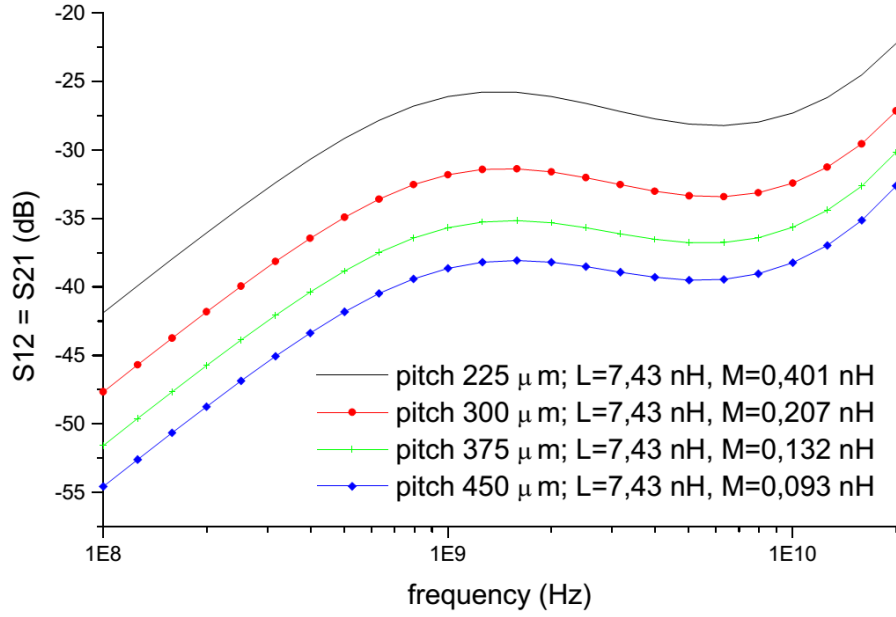


Figure 3.14. Dependence of the mutual coupling on the inductor-to-inductor distance (pitch).

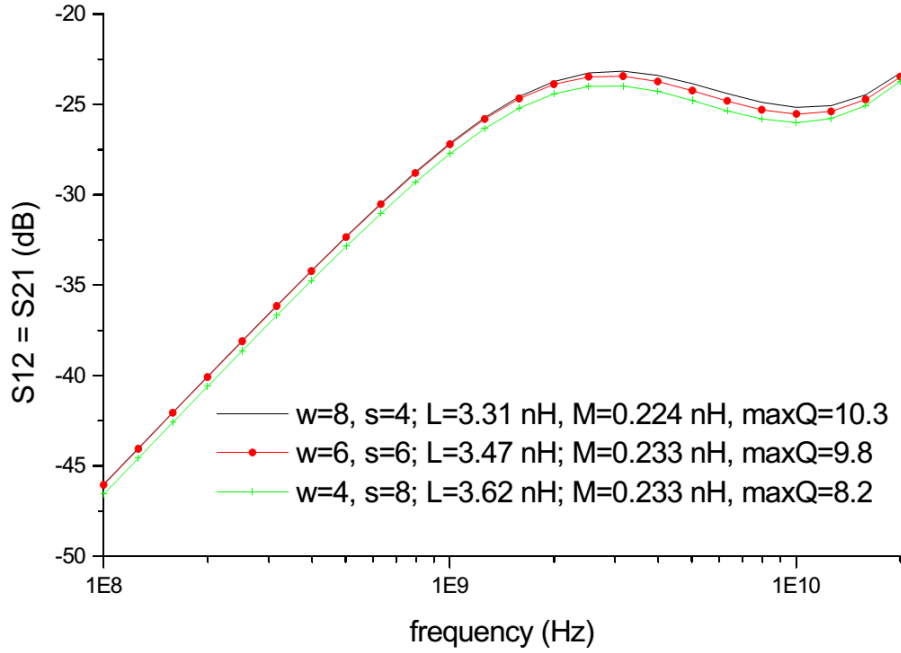


Figure 3.15. Dependence of the mutual coupling on the inductor parameter  $w/s$ , while maintaining the internal and external radii.

A layout choice that sometimes does not deserve attention is the relative orientation of the inductors. As a matter of fact, orientation must be defined relative to the directions of the current flowing along the inductors. We define "same orientation" when the currents, assumed to flow from the port terminal to the ground terminal, flow in the same direction. For example, the inductors shown in

Fig. 3.5 have the same orientation, since currents would flow counter-clockwise in both of them. By mirroring one of the inductors, we would obtain inductors with "mirrored orientation". Fig. 3.16 shows the simulation results of two different inductors, laid in both orientations. The "large" labeled inductor has 6.5 turns and internal radius of  $44\ \mu m$ , which produces a  $7.43\ nH$  self-inductance. The "small" labeled inductor has only 1.5 turns and internal radius of  $87\ \mu m$ , which produces a  $1.16\ nH$  self-inductance. It can be seen that about  $10\ dB$  lower coupling is expected when the orientation of the inductors is mirrored at least up to the slope change at frequency  $f_p$ , after which a resonance appears for the large inductor that even further reduces the coupling. Apparently this resonance does not appear in the small inductor, at least in the frequency range simulated. The results of the large inductor are consistent with those shown in [88] for two square inductors implemented in a GaAs substrate, including the resonance observed for the mirrored orientation.

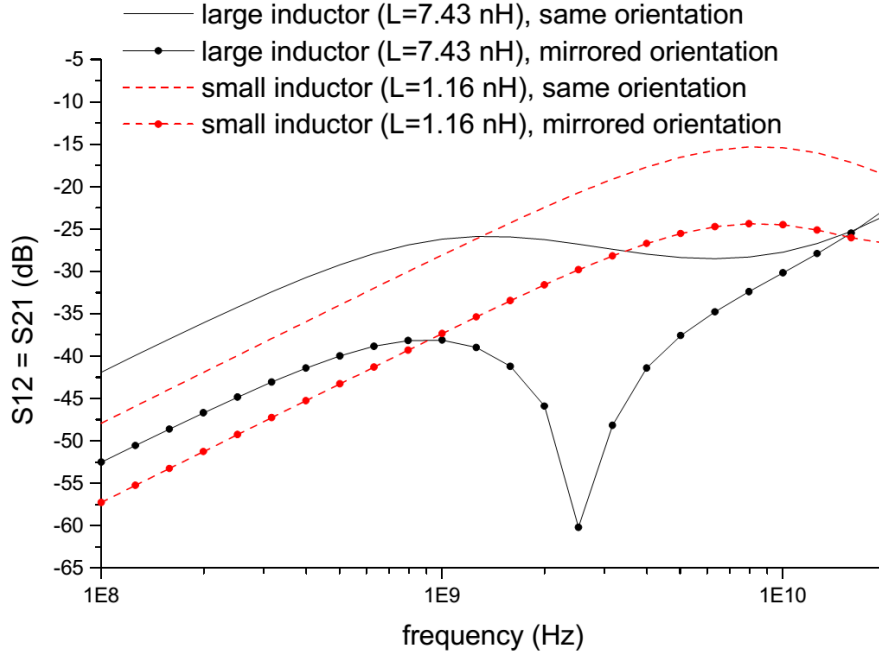


Figure 3.16. Dependence of the mutual coupling on the relative inductor orientation.

To complete this section, we want to quantify the relative importance of the EM coupling respect to the conductive coupling through the silicon substrate. Therefore, we compare the simulation of the two inductors described in the former section, laid in a silicon substrate ( $\rho=20\ \Omega\dot{c}m$ ,  $\epsilon_r=11.9$ ), against the simulations when the substrate is defined as a pure dielectric, i.e. its conductivity is forced to zero. Fig. 3.17 shows the results obtained. It can be verified that, for both inductors, the conductivity of the substrate has a minor impact on the coupling, and instead of contributing to increase coupling, it slightly decreases it. Therefore, it can be concluded that substrate coupling

between inductors is negligible in front of EM coupling. The substrate conductivity helps conduction to ground, and therefore slightly reduces the amount of signal coupled between inductors.

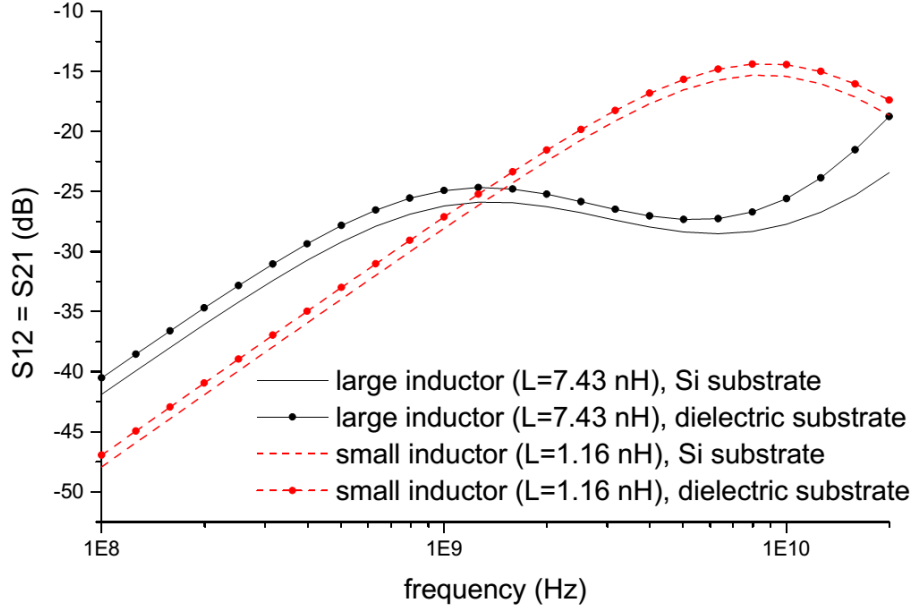


Figure 3.17. Comparison of mutual coupling between inductors laid in silicon versus dielectric substrate.

### 3.3.3 Experimental measurements

A test chip containing pairs of coupled inductors has been implemented in a  $0.35\ \mu\text{m}$  technology, with a thick top metal layer. Fig. 3.18(a) shows the layout of the implemented test structures. Inductor ends are connected to probe pads, and GSG passive probes have been used to measure mutual coupling  $S_{21}$  with a network analyzer, as depicted in Fig. 3.18(b). Inductor ends are connected as depicted in Fig. 3.5, i.e. one of the ends is grounded, while the other one is the access port. The chip is glued to a  $1\ \text{mm}$  thick glass support, thus isolating the silicon from the grounded chuck. Substrate is surface grounded with two rows of p-taps laid below the left and right pad set, in each test structure. Measurements were done in different chip samples, with coincident results.

The objectives of the measurements are, first, to experimentally verify the qualitative behavior observed with the EM Momentum simulations; second, to validate the simulations performed, i.e. to quantify the degree of matching on the  $S_{21}$  parameter between measurements and the simulation of the same test structures, and therefore quantify the error expected from the simulation results; and third, to test the efficacy of guard rings and patterned ground shields as techniques to decrease coupling. All measurements presented here have pad and probe parasitics de-embedded. The pad

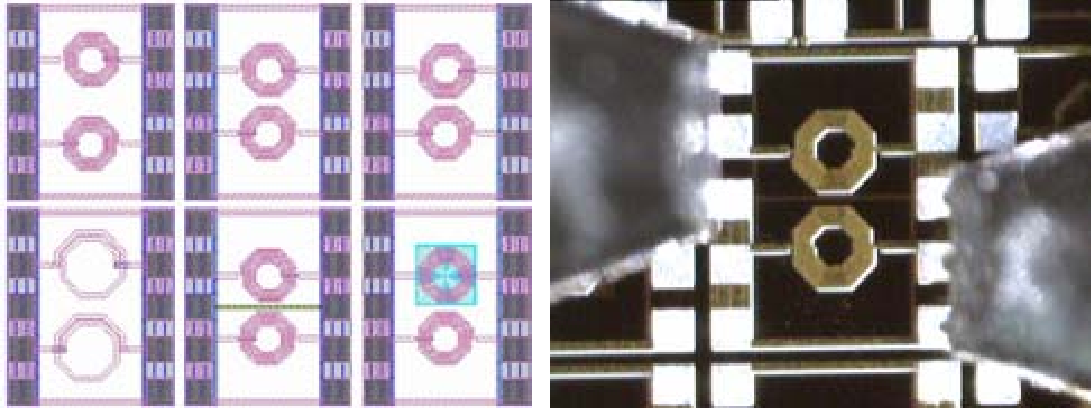


Figure 3.18. Layout of the test structures (a), and image of the measurement with GSG probes (b)

parasitics were obtained by measuring a test structure implementing an open, while the probe-to-pad impedance was obtained from a test structure implementing a short. Simulations presented in this section have also followed the same process, i.e., test structures were simulated including the pads (the full layout of the test structure was imported to Momentum), and pad parasitic were later de-embedded from the simulation results. These pad parasitics were obtained from a simulation of the test structure implementing an open. Fig. 3.19 shows the measurements of two coupled 6.5 turns,  $7.43\text{ nH}$  inductance with pitch  $225\text{ }\mu\text{m}$ , in both direct and mirrored orientations, and the comparison to the simulations. The layout of these inductors is thus exactly the same as the "large" inductors simulated in Fig. 3.16, and consequently the behavior observed matches those curves, including the resonance for the inductors laid in a mirrored orientation. It must be noted that all the presented simulations assumed a grounded reference at the chip backside, while in this section substrate is grounded with two rows of p-taps in the surface. This explains small differences that can be appreciated between the plots in Fig. 3.16 and Fig. 3.19. In any event, very good matching is observed between the measurements and the simulation results, which validates the dependencies predicted by the simulator in the previous section.

The measurement of coupling between small, 1.5 turn inductors is depicted in Fig. 3.20, compared to the large, 6.5 turn inductors. Small inductors are placed in a mirrored orientation, while their pitch is  $300\text{ }\mu\text{m}$ . Once again, simulations match perfectly the measured behavior with an error smaller than  $1\text{ dB}$  up to  $20\text{ GHz}$ . It can be checked that, even that the small inductor is placed in a mirrored orientation, no resonance appears in the frequency range measured, which confirms the prediction in Fig. 3.16. This confirms the validity of Momentum as a tool to evaluate coupling between integrated inductors, and the validity of the results obtained from the model.

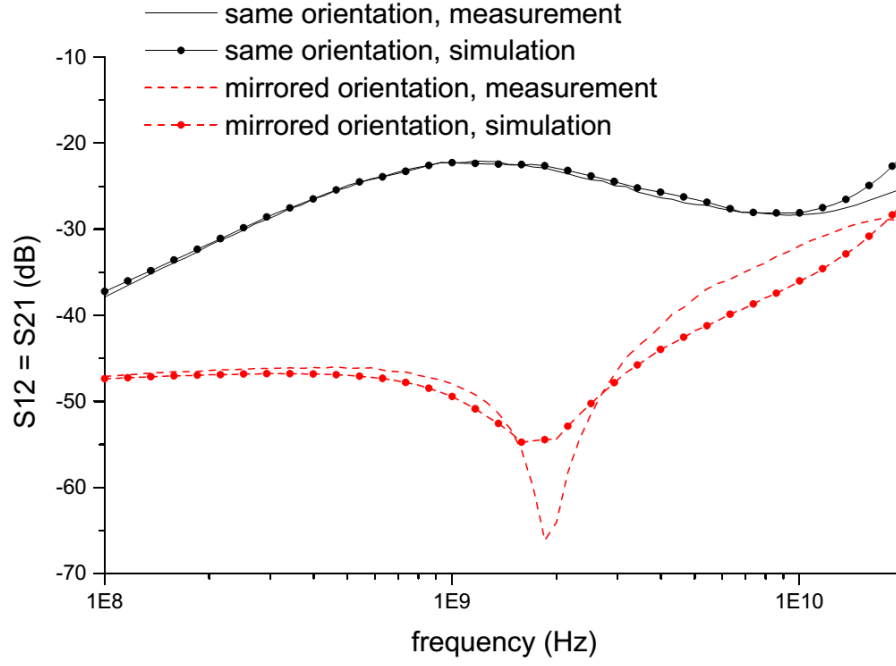


Figure 3.19. Measurements and simulations of 6.5 turn inductors, in different relative orientations.

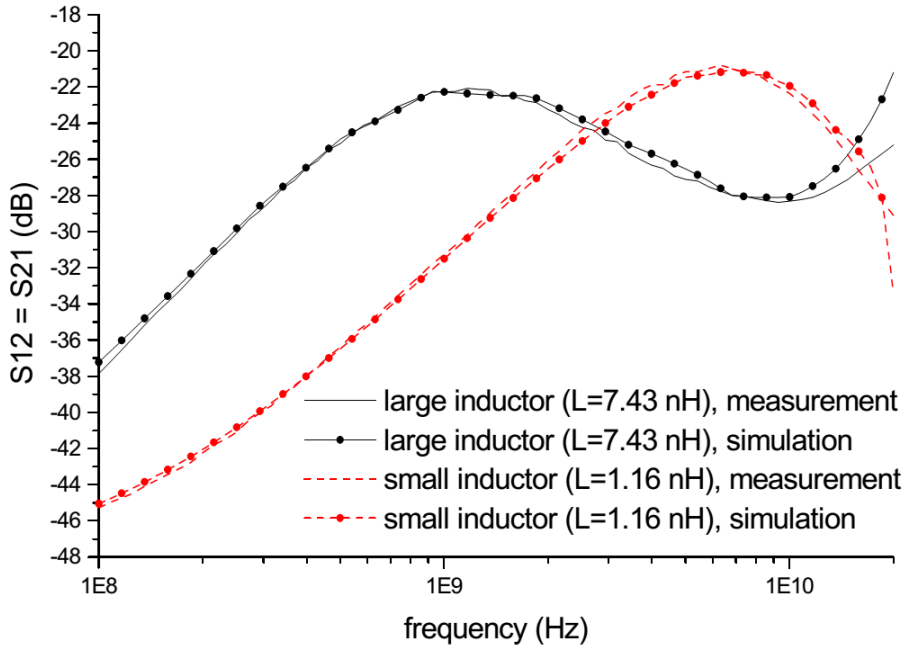


Figure 3.20. Measurements and simulations of coupled 1.5 turn inductors (small) and 6.5 turn inductors (large).

Finally, experimental results are presented of the performance of two techniques commonly proposed to reduce coupling. The first one is a grounded row of p-tap placed between the inductors, forming a separation wall. This row, together with the default rows of p-taps for substrate biasing, forms two guard rings that enclose both inductors at all their sides except the most external one. The

second technique to reduce coupling is a patterned ground shield placed below one of the inductors. This shield is implemented in polysilicon, laid in a radial pattern opened at the center and grounded at the inductor periphery. Both layouts can be appreciated in the lower right side of Fig. 3.18 (a). In all cases, inductors are placed in a mirrored orientation. Fig. 3.21 shows the measurements obtained. It can be observed how the effect of the grounded wall is a  $2.5\text{ dB}$  coupling reduction at low frequencies, while moving the resonance from  $2\text{ GHz}$  to  $4\text{ GHz}$ . The patterned ground shield does not provide significant coupling reduction at low frequencies, while it originates the appearance of different resonances, the first of which is already observed well below  $1\text{ GHz}$ . Above this frequency, the behavior of the coupling is quite erratic. Therefore, the use of patterned ground shields appears as a non-reliable measure to reduce coupling, while guard rings are a more effective measure.

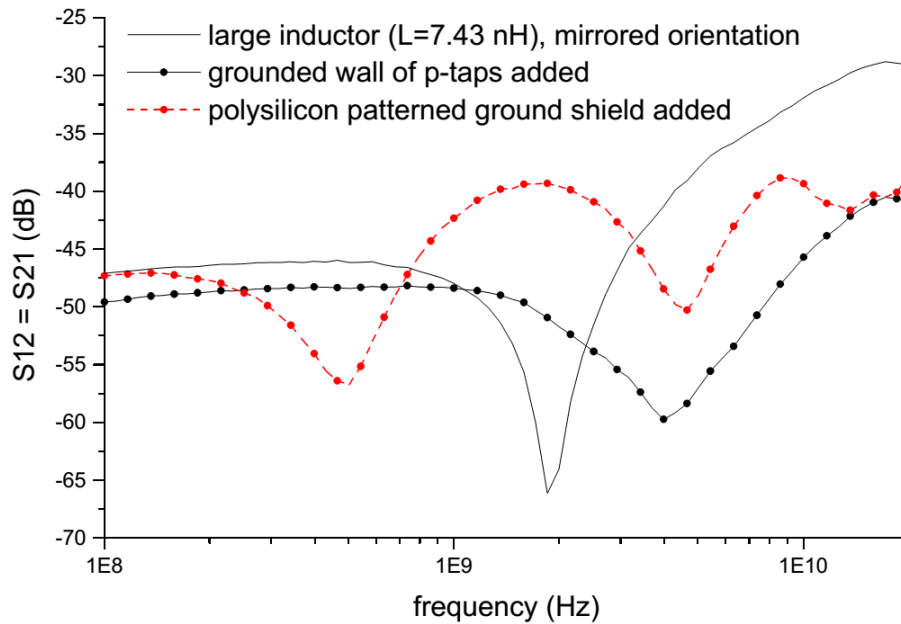


Figure 3.21. Measurements of the effect of inserting a grounded wall of p-taps between two mirrored inductors, versus the effect of placing a patterned ground shield below one of them.

### 3.4 Summary and conclusions

This chapter has evaluated two mechanisms that the noise has to couple between different areas of an integrated circuit:

- the coupling level between two substrate contacts due to the propagation of the noise through the substrate.

- the coupling level between two inductors. Especial attention has been taken to evaluate the role of the substrate in the coupling level.

Several test structures have been fabricated to empirically analyze these two issues. In both cases, the coupling level has been measured from very low frequencies up to  $40\text{ GHz}$ . This analysis has been focused in the evaluation of the different available options that a designer has to reduce the amount of noise that reaches a certain point of the circuit.

The noise propagation of the noise through the substrate has been evaluated using two direct contacts to the substrate. The measurements (together with simulations) have quantified the portion of the injected noise that reaches the other contact as a function of the noise frequency showing that this portion of noise is constant at low frequencies but it grows substantially at high frequencies. Several protection structures to minimize the noise reaching the victim contact have also been evaluated. These protection methods are:

- Distance
- P+ ring to GND
- N- ring to  $V_{dd}$
- P+ ring to GND and N- ring to  $V_{dd}$
- Triple wells
- Triple wells and P+ ring to GND

A common factor of all the analyzed protection structures is the loss of efficiency for frequencies beyond  $1\text{ GHz}$ . Experimental results have shown that a P+ grounded guard ring around a sensitive device provides the best protection against substrate noise, increasing, in the presented setup, the isolation against substrate coupling by  $30\text{ dB}$ . The distance between the victim and the aggressor has also shown to be an effective isolation method. The isolation grows with distance at low frequencies but it also losses efficiency as the frequency reaches the Gigahertz frequency range. Another conclusion obtained in this analysis is that the design of the ground return path is critical to provide a high level of isolation.

Regarding the coupling between spiral inductors, a complete study, including analysis, modeling and experimentation, has been carried out in order to understand the factors that favor mutual

coupling between inductors, including the role that the substrate has in this coupling. Measurements and simulation have shown that coupling between spiral inductors at low frequencies increases at a rate of  $20 \text{ dB/dec}$  with an exclusive dependence with the mutual inductance  $M$ . At some frequency,  $f_p$ , determined by the inductors self inductance, the coupling trend changes. After this frequency, coupling depends on the ratio  $M/L^2$ . A second coupling trend change is found at a higher frequency,  $f_z$ , where the substrate plays an important role. Again, the coupling level at high frequency is much more relevant than at low frequency.

A simplified model has been deduced to obtain some insight regarding the most relevant coupling mechanisms between inductors. This simplified model has shown to be effective to model the coupling up to  $f_p$ , while a distributed model is necessary to predict coupling behavior above that frequency limit.

The measured test structures have shown correlation between the coupling level and the physical parameters of the inductors. For example, the distance between the inductors is a very efficient parameter, over the whole frequency range, to increase the isolation. Particularly interesting is the fact that, even if the pitch is fixed, coupling will increase importantly if the inductor size increases, because of the shorter distance between outer edges. An interesting test, very related with the rest of this thesis, has included a P+ guard ring between the inductors. Measurements have shown that this ring reduces the coupling level between the inductors, proving that the substrate has a very important role in the coupling between inductors.



## **Chapter 4**

# **Effect of substrate noise on the LC-VCO performance degradation.**

### **4.1 Introduction and objectives**

The state-of-the art review in Chapter 2 has detailed observations of performance degradation in LC-VCOs produced by the presence of high-frequency tones in the substrate, which can ultimately lead to complete system malfunction. This chapter analyzes, from an empirical point of view, the effect of a HFSN tone in the output spectrum of an LC-VCO and its dependence with the characteristics of both, the noise and the oscillator.

An integrated circuit has been designed in order to experimentally observe this effect, and proceed to a systematic analysis to obtain information beyond that already published in the literature. The circuit is designed with the purpose of analyzing the effect on the output waveform of an LC-VCO of a tone injected in the substrate with a frequency close to the natural oscillator frequency. This empirical approach will be the first step in the deep analysis that will be done in the following chapters.

The designed integrated circuit is presented in section 4.2 while the measurement results are analyzed in section 4.3. The possible causes and interaction effects are finally presented in section 4.4.

## 4.2 Test setup description

An experiment setup has been designed in order to emulate the scenario where an LC-VCO (victim) is perturbed by a high power RF system (aggressor), like a power amplifier, that leaks some energy to the common silicon substrate at a frequency close to that of the LC-VCO. The experiments should show if the leaked energy can travel through the substrate from the aggressor to the victim, and degrade the performance of the LC-VCO. The experiment replaces the aggressor with a pad connected to the substrate, so that high frequency signals, with controllable power and frequency, can be injected into the substrate. A full working  $7\text{ GHz}$  LC-VCO has been designed to check the performance under the effect of the high frequency substrate injected noise.

### 4.2.1 Test chip description

A  $7\text{ GHz}$  LC-VCO has been fabricated in a CMOS  $0.18\text{ }\mu\text{m}$  technology. The resonant tank has been designed using a differential inductor and two parallel varactors. The full layout is completely symmetrical in order to avoid output unbalance. Two NMOS transistors connected in a cross coupled scheme are used to form the required negative resistance on the tank. The current biasing source is also built with two PMOS transistors to allow a symmetrical layout. The bias current flowing through the PMOS transistors can be tuned through  $-V_{bias}$ . Two output buffers have been used to provide a suitable  $50\text{ }\Omega$  output impedance. Fig.4.1 shows a micro photography of the chip.

The VCO has a nominal power consumption of  $23\text{ mW}$  from a  $1.8\text{ V}$  supply voltage using a  $V_{bias} = 0.8\text{ V}$ . The oscillation frequency can be tuned thanks to a control voltage  $-V_c$  connected to the tank varactors. The output frequency sweeps from  $6\text{ GHz}$  to  $8\text{ GHz}$  with a maximum sensitivity to the control voltage of  $2\text{ GHz/V}$ . The following graphs summarize the measured characteristics of the LC-VCO. The oscillation frequency and the oscillation amplitude for a complete sweep of  $V_c$  is shown in Fig.4.2. Fig.4.3 shows the relationship between current consumption and bias voltage for  $V_c = 1.8\text{ V}$ . Fig.4.4 and Fig.4.5 show the oscillation power and frequency for three different control voltages.

Substrate noise injection pads have been included in the layout design in order to directly inject the noise signal into the substrate. There are 4 different injection points to check the effect of distance and orientation. The injection pads can be appreciated in Fig.4.1. The interfering noise is generated with a single tone signal generator, and it is injected in the substrate through a GSG RF

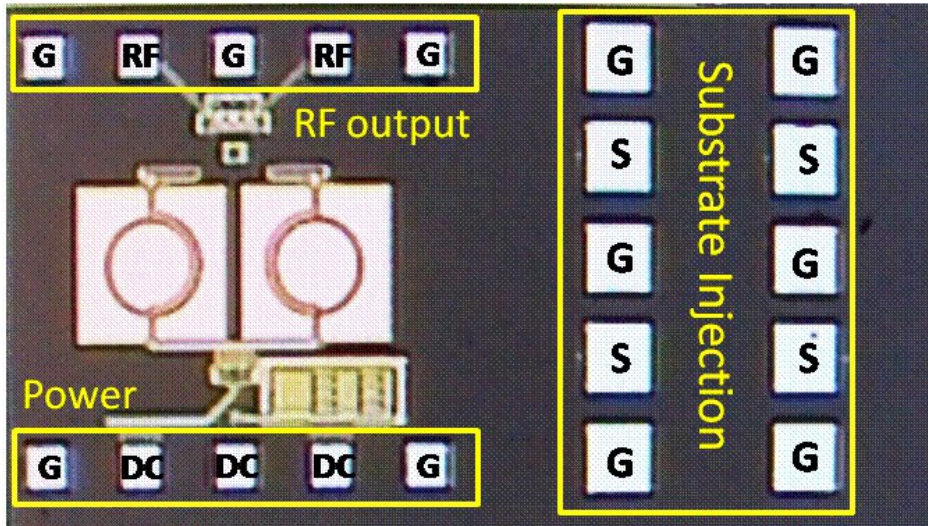


Figure 4.1. Test chip micro photography

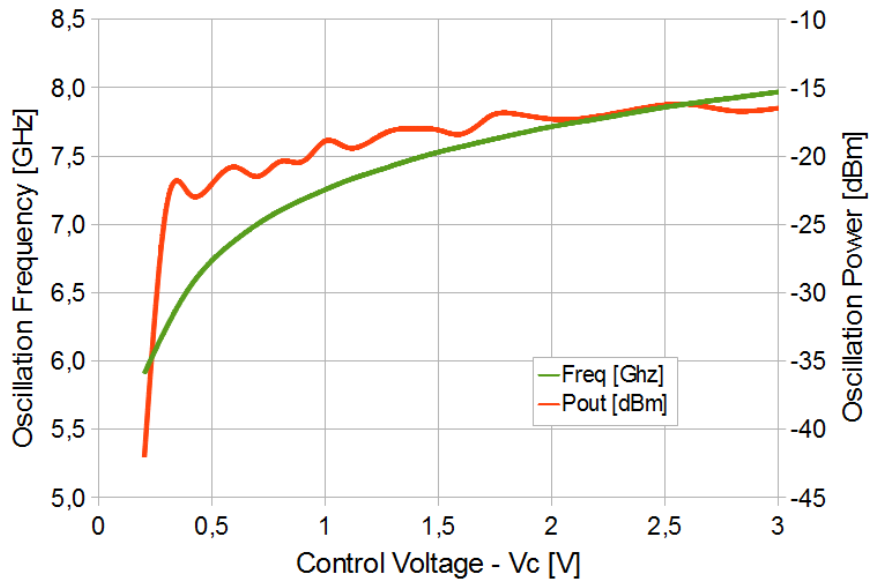


Figure 4.2. Oscillation frequency and output power vs. Control Voltage ( $V_c$ ) for  $V_{bias} = 900mV$

probe contacting a pad that is capacitively coupled to the substrate. The RF outputs, DC and power pads have been wire bonded to a PCB (Chip on board).

#### 4.2.2 Measurement process

In order to perform the measurements a FR4 PCB has been designed and fabricated. All the DC signals (Control voltage, bias voltage and power supply signals) have been wire bonded to the PCB to allow the connection of external DC low noise power supplies. The RF output pads of the

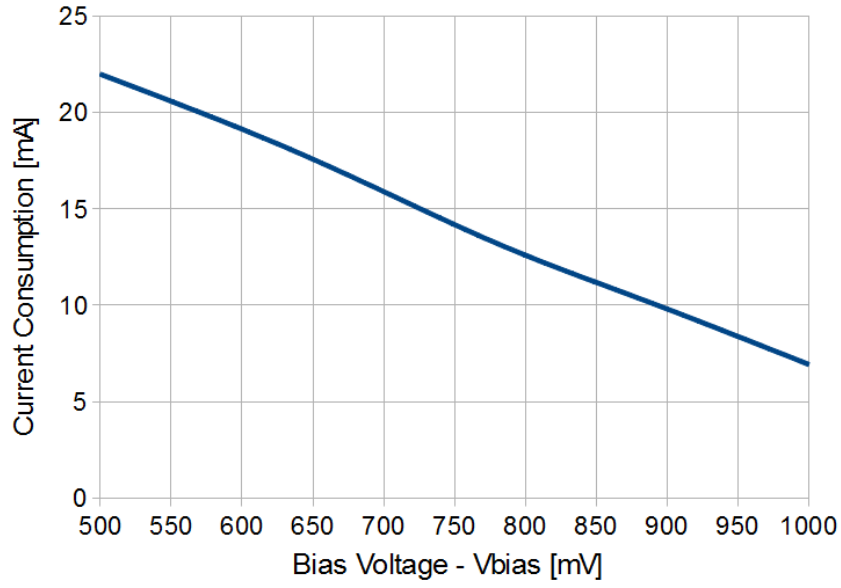


Figure 4.3. Current consumption vs. bias Voltage for  $V_c = 1.8V$

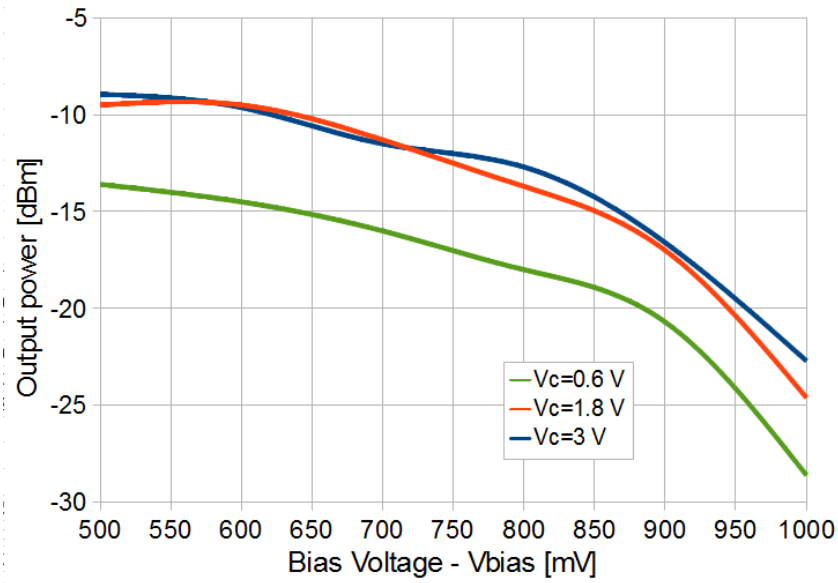


Figure 4.4. Oscillation power vs. Bias Voltage for  $V_c = 0.6V, 1.8V, 3.0V$

LC-VCO have also been wire bonded to the PCB and routed to SMA connectors. An image of both, the bonding wires and the designed PCB is shown in Fig.4.6. The output signals of the LC-VCO are decoupled and combined using a 2-10  $GHz$  balun. The output of the balun is connected to a Rohde&Schwarz FSQ26 Signal analyzer.

The substrate noise injection pads have not been wire bonded, they will be directly accessed at IC level using a GSG RF 100  $\mu m$  pitch picoprobe.

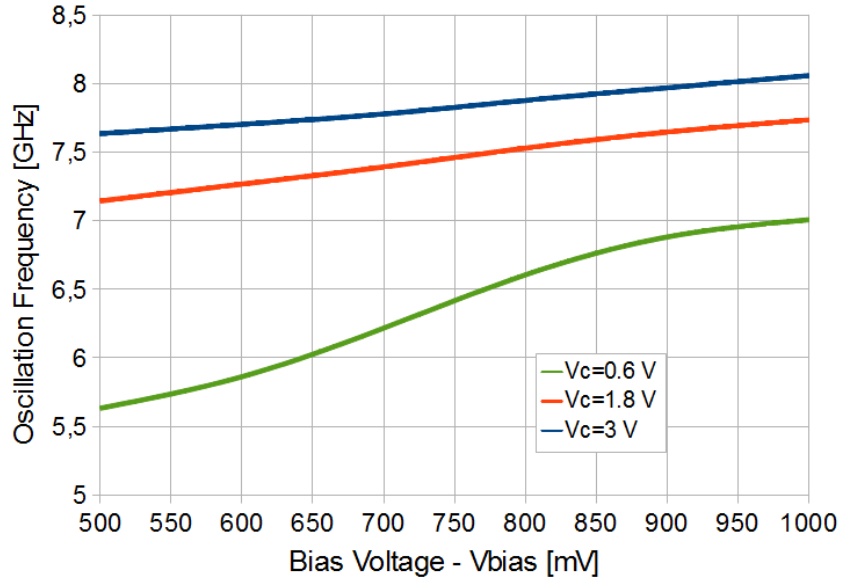


Figure 4.5. Oscillation Frequency vs. Bias Voltage for  $V_c = 0.6V, 1.8V, 3.0V$

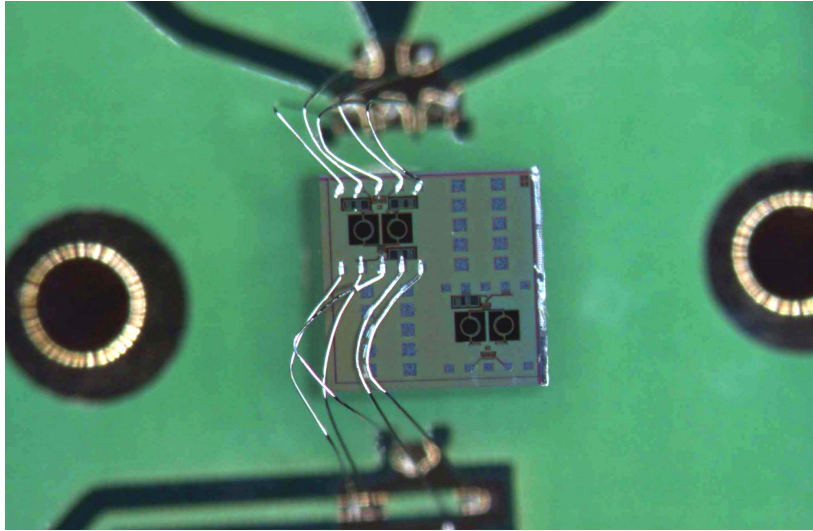


Figure 4.6. 7 GHz IC wirebonding to the measuring PCB

### 4.3 Effect of HFSN on the VCO output spectrum

The injection into the substrate of a sinusoidal tone with a frequency close to the fundamental output frequency of the VCO,  $\omega_o$ , generates two symmetric sideband spurs, one at the injected frequency,  $\omega_i$ , and another one at  $2\omega_o - \omega_i$ . Fig.4.7 shows a typical observation of this effect. An important characteristic of the sideband spurs is that they have approximately the same amplitude. As the frequency offset is increased, the amplitude of the spurs falls at a rate of  $20 \text{ dB/dec}$ . This effect is reflected in Fig.4.8, which shows the measured relative amplitude (referred to the fundamental

oscillator amplitude) of the sidebands for frequency offsets from  $2\text{ MHz}$  up to  $500\text{ MHz}$ . Fig.4.8 shows that the sideband at  $2\omega_o - \omega_i$  consistently follows the  $20\text{ dB/dec}$  dependence. The amplitudes of both sideband is the same for most of the frequency offsets except for very low offsets, where the amplitude of the  $\omega_i$  sidebands grows, and for very high offsets, where the sideband at  $\omega_i$  saturates.

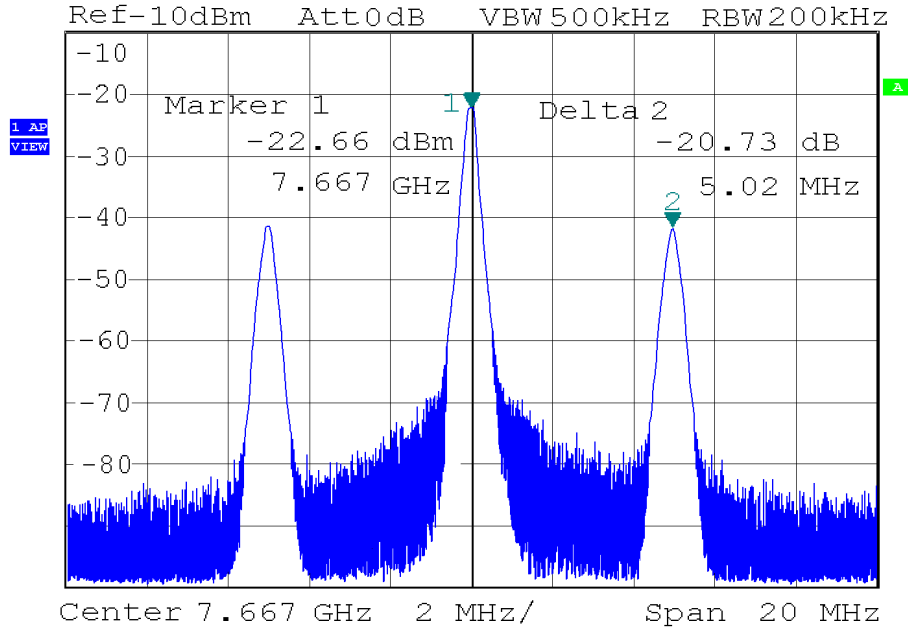


Figure 4.7. Output spectrum of the VCO perturbed by a substrate coupled noise at a  $5\text{ MHz}$  frequency offset from the carrier

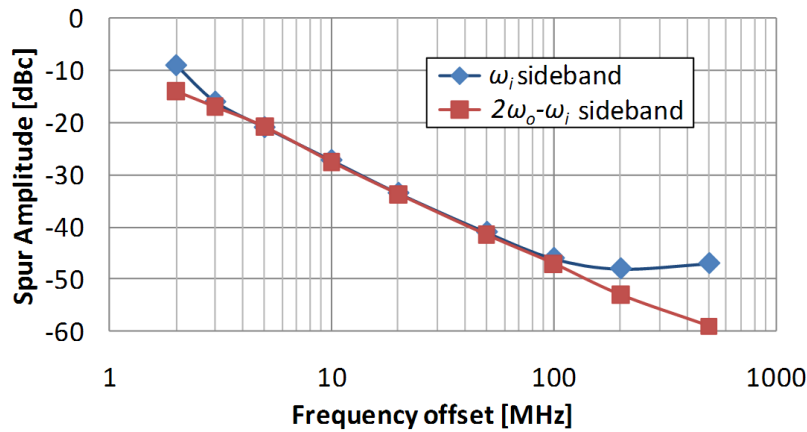


Figure 4.8. Spur amplitude for different frequency offsets

Extra information may be obtained by measuring the effect of the HFSN when the oscillator is forced to stop oscillation. The oscillation has been switched off reducing the biasing current below the minimum current that makes oscillation possible. The buffers are working at the same operating

point as they are independently powered and biased. The effect of the HFSN on the output spectrum of the system when the LC-VCO is not oscillating shows that the amount of noise that reaches the oscillator output has a barely perceptible dependence with the frequency. The measured amplitude of the noise tone at the VCO output is around  $-70\text{ dBm}$  (see Fig.4.9). This power is coupled from the substrate into the LC-VCO and also into the output buffers. Some conclusions are obtained from this test. On one hand, the amplitude of the tone is constant when the LC-VCO is off suggesting that, when the LC-VCO is on, there should be an interaction between the HFSN and the oscillator in order to explain the  $20\text{ dB/dec}$  effect and the appearance of a second sideband. Some possible alternative explanations which could explain the  $20\text{ dB/dec}$  dependence are ruled out due to the results of this test, as for example that the amount of noise reaching the tank depends on the tank impedance, which is very low when the frequencies are close to the resonance frequencies. On the other hand, this test shows that the power measured at  $\omega_i$  when the VCO is on is formed by two components, the interaction between the noise and the VCO and the direct coupling on the tank and on the output buffers. This conclusion explains the causes of the saturation of  $\omega_i$  sideband power for very high frequency offsets, as shown in Fig. 4.10. The reasons and mechanisms regarding the small frequency offset amplitude difference will be analyzed in chapter 5.

The dependence of the sideband amplitude with the power of the injected HFSN has also been

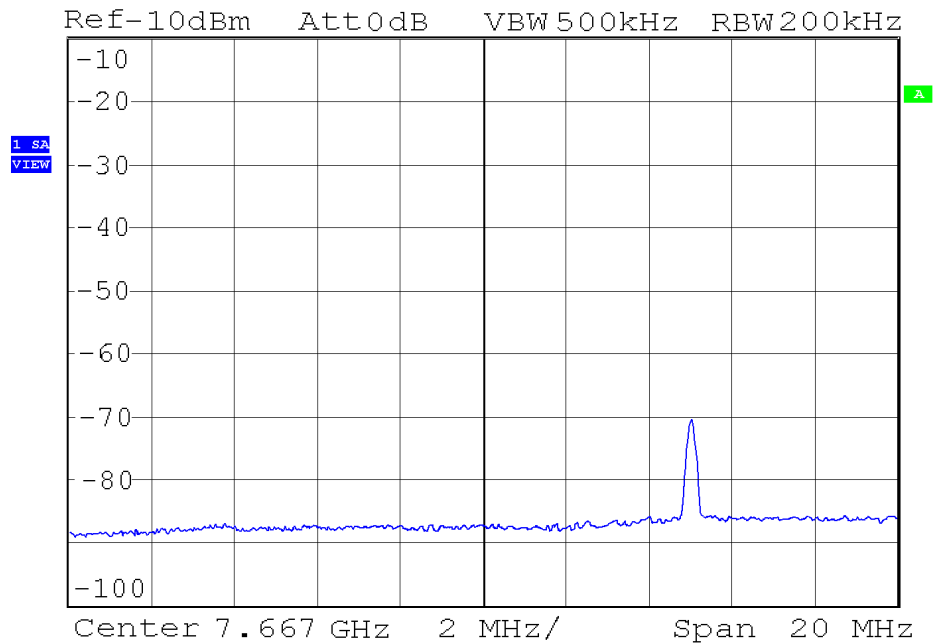


Figure 4.9. Output spectrum with HFSN injected and the VCO not oscillating

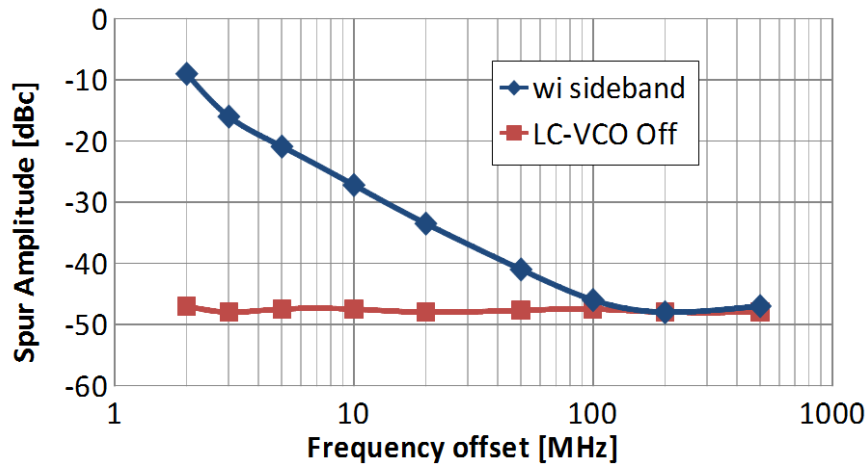


Figure 4.10. Comparison between the sideband amplitude with and without VCO oscillation

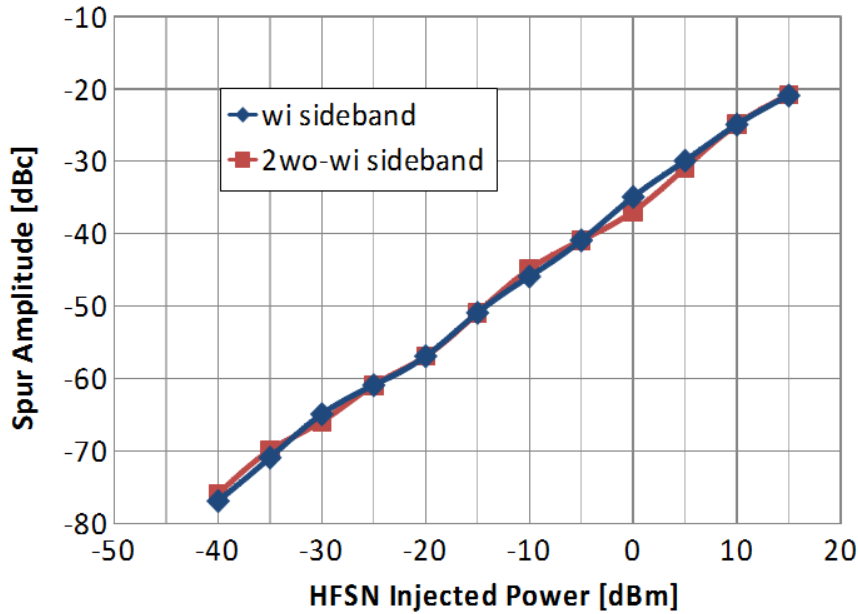


Figure 4.11. Comparison between the sideband amplitude and the HFSN amplitude

analyzed. Fig.4.11 shows the measured amplitude of the spurs a function of the injected HFSN power. Fig.4.11 shows a clear proportionality between both amplitudes, meaning that an increase of, for example, 10 *dB* on the HFSN would have an impact of 10 *dB* in the amplitude of the sidebands.

In order to gain more insight of the interaction between the HFSN and the VCO, the occupied bandwidth of each of the sidebands has also been analyzed. It has already been shown in Fig.4.7 that the injection of HFSN generates two sidebands around the fundamental VCO oscillation frequency. The measurements shown in Fig.4.7 have been done using a very high resolution bandwidth in the setup of the spectrum analyzer. As the resolution bandwidth is higher than the occupied bandwidth of



each of the tones, the spectrum analyzer accurately measures all the power of each of the sidebands but all the info about the occupied bandwidth gets hidden. In order to observe the occupied bandwidth, the resolution bandwidth of the measurement equipment should be reduced and a "max-hold" measurement should be performed. Fig.4.12 shows the results of this measurement. The fundamental oscillation of the VCO in that particular case has an occupied bandwidth of about  $3.5\text{ MHz}$ . This means that the oscillator is not perfectly oscillating in a pure frequency but slightly changing around a central oscillation frequency. The phase noise of the LC-VCO and the noise on the power lines can modify the oscillation frequency. The sideband at  $\omega_i$  shows a very small occupied bandwidth, it is actually limited by the spectrum analyzer resolution bandwidth. The HFSN is generated with a very precise and accurate RF generator which can generate tones with very low occupied bandwidth. Finally, the sideband at  $2\omega_o - \omega_i$  shows an occupied bandwidth around  $7\text{ MHz}$ , so, twice the occupied bandwidth of the VCO. The causes and consequences of the occupied bandwidth of each sideband will be further analyzed in the following chapters.

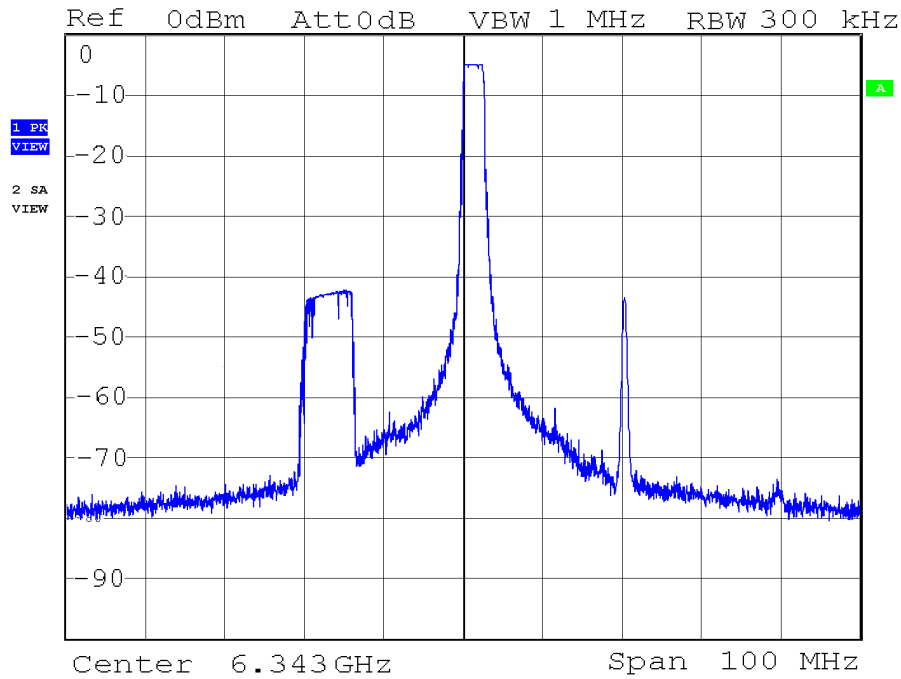


Figure 4.12. Output spectrum of the HFSN perturbed VCO showing the occupied bandwidth of each of the sidebands

The effect of the oscillation amplitude on the robustness of an LC-VCO to HFSN has also been analyzed. The performed measurements show that an increase of the power consumption of the LC-VCO increases the oscillation amplitude (see Fig.4.13) but it does not significantly modify the absolute amplitude of the sidebands. Consequently, the relative amplitude of the sidebands is reduced

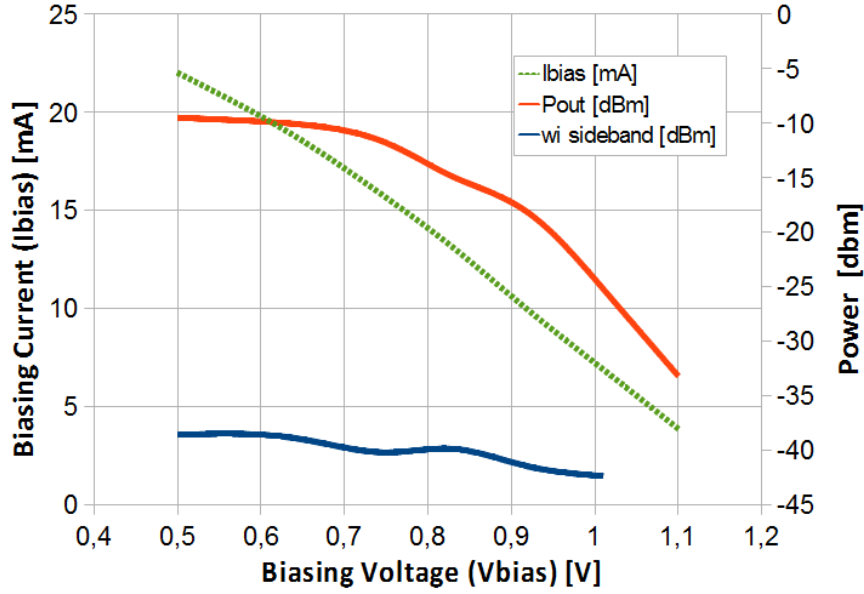


Figure 4.13. Comparison between the sideband relative amplitude and the VCO oscillation amplitude due to the increased oscillation amplitude. Fig.4.13 shows the amplitude of both the LC-VCO output and the  $\omega_i$  sideband for different  $V_{bias}$  voltages and, so, different LC-VCO power consumption.

All the measurements and presented characteristics of the HFSN perturbed VCO have been confirmed for different oscillation frequencies and different injected power in several different dies.

#### 4.4 Empirical analysis of the causes of the VCO output degradation

As a summary of the analysis presented in 4.3, the measurements have shown that a high frequency tone injected in the substrate generates two symmetric sidebands in the output spectrum of the perturbed VCO, one at the injected frequency,  $\omega_i$ , and another one at  $2\omega_o - \omega_i$ . The sideband have approximately the same amplitude. As the frequency offset is increased, the amplitude of the spurs falls at a rate of  $20 \text{ dB/dec}$ . The amplitude of the sidebands is proportional to the amplitude of injected tone. The relative amplitude of the sidebands is proportional to the oscillation amplitude of the VCO. Attenuation or amplification of the output signal does not modify the relative amplitude of the sidebands. The sideband appearing at the injected frequency has the same bandwidth than the injected tone while the sideband at  $2\omega_o - \omega_i$  has an occupied bandwidth around twice the occupied bandwidth of the VCO oscillation. This section will analyze all the measurements presented in 4.3 in order to discuss, from an empirical point of view, the possible interaction mechanisms that can be responsible of the presented effects.

#### 4.4.1 Frequency mixing

A possible explanation of the generated spurs, especially the one at  $2\omega_o - \omega_i$ , has been previously proposed in the literature [11], [48] as an intermodulation between the VCO output and the injected tone due to the non-linearities of the resonant tank.

When a tone signal is applied to a non-linear element additional signals are generated at multiples of the original frequency (harmonics). When a second tone is present and both tones are close together in frequency, some of the sum and difference frequencies, called intermodulation products, may lay very close to the original input frequencies. The particular scenario with a second tone can be analyzed with simple mathematical approach provides a lot of insight The transfer function can be described using a Taylor series:

$$P(s) = a_0 + a_1 \cdot s + a_2 \cdot s^2 + a_3 \cdot s^3 + \dots \quad (4.1)$$

where  $s$  is the dual tone signal with amplitudes  $A_1, A_2$  and frequencies  $f_1, f_2$ :

$$s(t) = A_1 \cdot \cos(2\pi \cdot f_1 + \varphi_1) + A_2 \cdot \cos(2\pi \cdot f_2 + \varphi_2) \quad (4.2)$$

After some calculation, one may obtain the frequency and amplitude of the generated harmonics.

Type of Intermodulation	Harmonic Frequency	Amplitude
Second Order	$f_1 + f_2$	$a_2 \cdot A_1 \cdot A_2$
	$f_1 - f_2$	$a_2 \cdot A_1 \cdot A_2$
Third Order	$2f_1 + f_2$	$a_3 \cdot A_1^2 \cdot A_2$
	$2f_1 - f_2$	$a_3 \cdot A_1^2 \cdot A_2$
	$f_1 + 2f_2$	$a_3 \cdot A_1 \cdot A_2^2$
	$f_1 - 2f_2$	$a_3 \cdot A_1 \cdot A_2^2$

Table 4.1. Frequency and amplitude of the generated second and third order harmonics.

Table 4.1 shows that one of the 3rd intermodulation products falls in the mirror sideband observed in the previous measurements,  $2f_o - f_i$ , but the calculated amplitude does not fit with those measurements. First, the amplitude of the intermodulation product is independent of the offset frequency (20dB/dec measured). Second, the amplitude is different from the noise amplitude (same

amplitude measured) . Finally, it has a quadratic dependence with the oscillation amplitude (linear dependence measured).

It is quite save to conclude that the effect of intermodulation cannot explain the observed characteristics of the sideband spurs.

#### 4.4.2 Frequency pulling

An alternative explanation for the sidebands is possible when the effects of HFSN on VCOs are analyzed from the perspective of an injection locked oscillator (ILO), where the injected signal is small and not too close to the VCO output. Under these circumstances, the injected signal cannot lock the VCO but is enough to perturb its output spectrum.

Back in 1946, R. Adler [89] described and formulated the behavior of locked and unlocked ILOs. Subsequently, his work was extended by H. Stover [90] and M. Armand [91] and more recently by B. Razavi [49]. As described in these works, injection locking is a common characteristic of free running oscillators. The natural oscillation frequency of the oscillator can be modified by an external signal, forcing the oscillator to oscillate (lock) at the frequency of the external signal. A diagram of this effect, is shown in Fig.4.14.

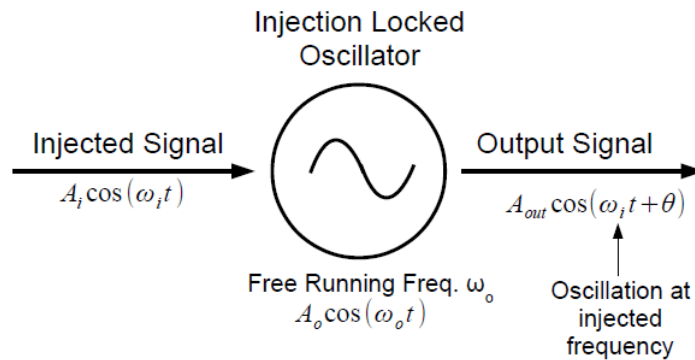


Figure 4.14. Oscillator Injection locking effect diagram.

Injection locking is only possible under determined characteristics of both the free running oscillator and the injected signal. As a rule of thumb, locking is only possible when the injected signal has an amplitude similar to the free running oscillator and both frequencies, injected frequency and free running frequency, are very close to each other. When these conditions are not met, the injected signal can still modify the instantaneous phase of the oscillator, and consequently, its instantaneous

frequency. So, the free running oscillator does not lock to the injected frequency but it is affected by it, this effect is known as frequency pulling. An early experimentation, published by H. Stover back in 1966, of the locking and pulling effect on the output spectrum of an oscillator is shown in Fig.4.15 [90].

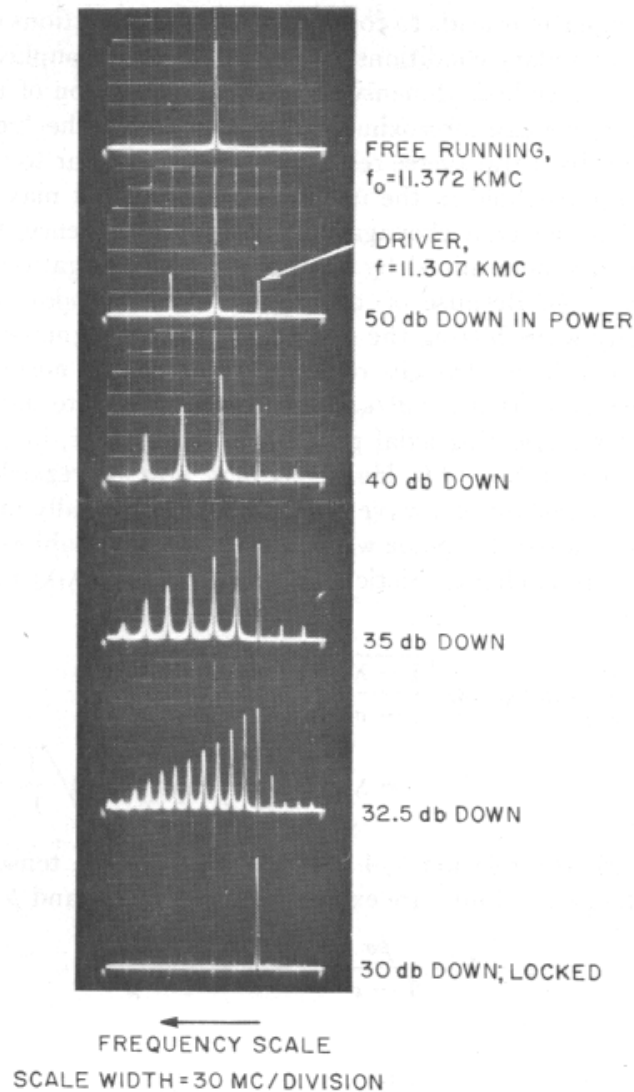


Figure 4.15. Output spectra of a driven tunnel diode oscillator, locked and unlocked [90].

The top image on Fig.4.15 shows the output spectrum of the oscillator without any noise injected. The oscillator is oscillating at  $11.372\text{ GHz}$  ( $11.372\text{ kMc}$ ). A  $50\text{ dBc}$  tone is injected with a frequency offset of  $0.035\text{ GHz}$ , shown in Fig.4.15-b. In this particular case, the injected signal is small compared to the oscillator signal and its frequency is relatively far from it, the output of the oscillator is modulated in frequency due to the frequency pulling effect [90]. The output spectrum of the oscillator under these circumstances presents two symmetric sidebands with the same ampli-

tude separated from the VCO fundamental  $\omega_o$  by an offset equal to  $\omega_o - \omega_i$ , exactly as observed in Fig.4.7. As the amplitude of the injected signal increases the pulling effect becomes stronger. The VCO frequency is slightly shifted towards the injected signal and several sidebands appear in its opposite side (Fig.4.15-c-d-e). In this situation, a slight reduction of the offset or a small increase on the injected power will force the VCO to lock to the injected signal, as shown in Fig.4.15-f, where the free running oscillator is now working as an ILO and so, oscillating at the same frequency as the injected signal.

The behavior reported in Fig.4.15 suggests that a possible explanation for the HFSN effects measured in section 4.3 is that the LC-VCO reacts as an ILO, before locking. In order to confirm this, an experiment has been carried out in our test chip, where a high power (15 dBm) has been injected in the substrate with a frequency offset that has been gradually reduced. This experiment wants to confirm that an LC-VCO can behave like an unlocked ILO. Fig.4.16-a shows the LC-VCO freely oscillating without HFSN. Fig.4.16 also shows the output spectrum of the VCO when a 15 dBm noise is injected in the substrate with frequency offsets of 5 MHz (Fig.4.16-b), 2 MHz (Fig.4.16-c) and 0.5 MHz (Fig.4.16-d). The output spectrum of the free running LC-VCO shows two sidebands with the same amplitude when the 5 MHz HFSN tone is injected. As the frequency offset is reduced, the amplitude of the sidebands grows at a rate of 20 dB/dec. Fig.4.16-c shows the effect of a 2 MHz frequency offset HFSN tone in the LC-VCO. The output frequency of the VCO has been pulled around 0.5 MHz towards the noise signal, which is the only spur on the left side of the VCO signal. On the right side, several spurs have been generated by the pulling effect. If the frequency offset is further reduced, the VCO gets locked to the noise tone. This effect shown in Fig.4.16-d, where the LC-VCO is oscillating at the injected HFSN. Finally, Fig.4.17 shows the measured locking range for different injected noise power levels. It can be seen that the higher the injected power, the higher the locking range.

The comparison between Fig.4.15 and Fig.4.16 shows that the output spectrum of the designed LC-VCO matches that of an unlocked ILO when a tone is injected in the substrate at a frequency very close to the free running oscillation frequency of the LC-VCO. The LC-VCO may be suffering from frequency pulling and frequency locking due to the noise signal traveling through the substrate.

In order to check that last proposed statement, the analysis of the performance degradation of the LC-VCO due to HFSN shown in section 4.3 can be done from the new ILO perspective. So, is it

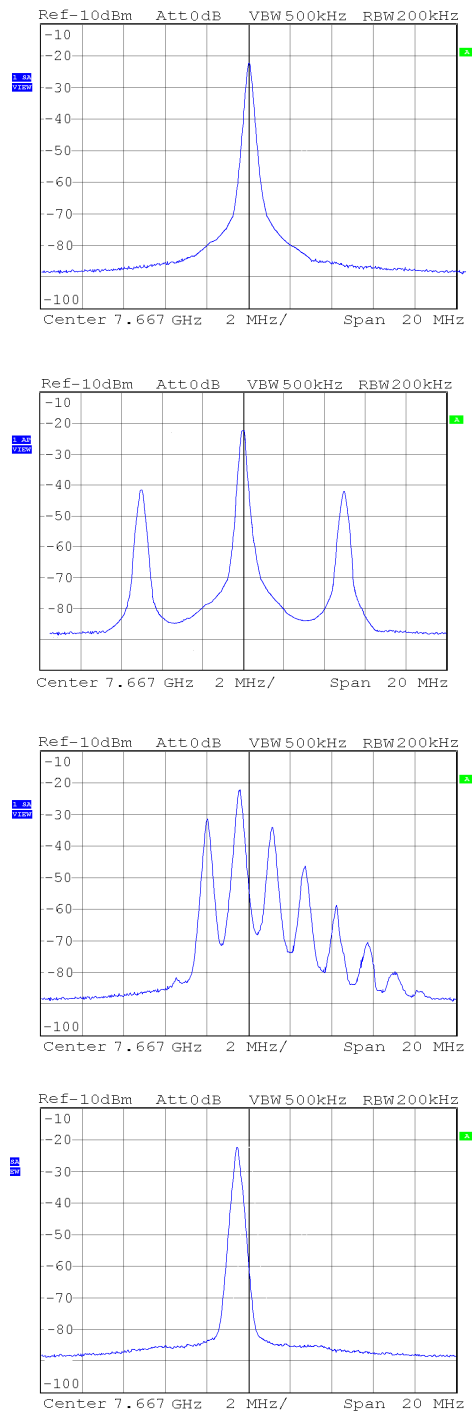


Figure 4.16. Measured output spectrum of the LC-VCO for different offset frequencies

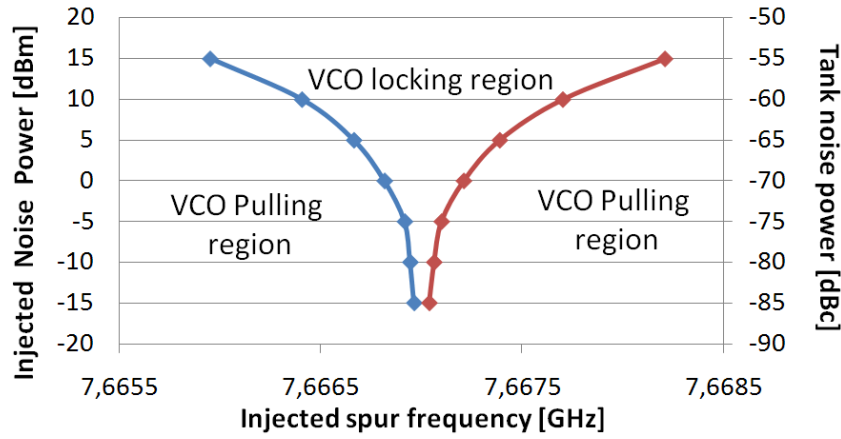


Figure 4.17. Measured locking range for different substrate noise power

possible to justify that the measurements presented in section 4.2.2 are caused by the pulling effect of the HFSN?

An ILO suffers from frequency pulling when the injection signal is too weak or too far from the free running oscillation frequency [89], [90]. The free running oscillator is frequency modulated by the injected signal. It has been proposed that the same effect takes place on an LC-VCO affected by a HFSN. The output spectrum of the HFSN affected LC-VCO shown in Fig.4.7 can be interpreted as a frequency modulation of the LC-VCO output. The carrier signal, with amplitude  $A_o$  and frequency  $\omega_o$ , is frequency modulated by a sine tone of frequency  $\omega_m = \omega_o - \omega_i$  and amplitude  $A_m$ . The output spectrum of this frequency modulation shows the carrier frequency,  $\omega_o$ , with two sidebands. Each sideband pair is symmetrically located around the carriers frequency,  $\omega_o$ , and separated from the rest frequency by integral multiples of the modulating frequency,  $n \cdot \omega_m$ , where  $n = 1, 2, 3$ . According to the performed measurements, most of the energy caused by the modulation lays in the first ( $n=1$ ) sidebands as they are the only one pair of sidebands with appreciable power. This type of FM signal meets the definition of narrow-band FM (NBFM) [92]. The typical output spectrum of a NBFM signal is shown in 4.18. The time domain behavior follows the equation<sup>1</sup>:

$$y(t) = A_o \cos(\omega_o t + \beta \cos(\omega_m t)) \quad (4.3)$$

<sup>1</sup> A detailed mathematical analysis of the FM approximation will be developed in chapter 5



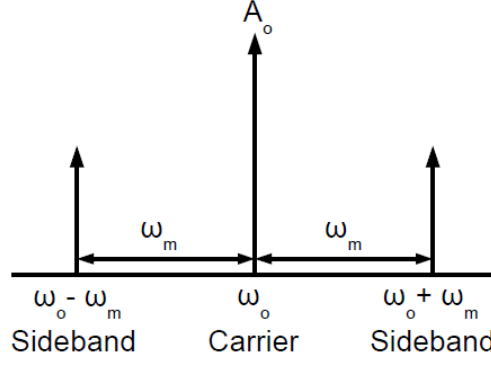


Figure 4.18. Diagram of the output spectrum of an narrow band FM modulated signal.

For a NBFM, 4.3 shows that the amplitude of the sideband pairs is proportional to the index of modulation,  $\beta$  which is defined as [92]:

$$\beta = \frac{\Delta\omega}{\omega_m} = \frac{\Delta\omega}{\omega_o - \omega_i} \quad (4.4)$$

where,  $\Delta\omega$  represents the maximum deviation of the instantaneous frequency from the carrier frequency. From a very intuitive point of view, frequency modulation converts a deviation of the modulation signal amplitude into a deviation of the carrier frequency, consequently, the maximum deviation of the carrier frequency should be proportional to the maximum amplitude of the modulation signal,  $A_m$ .

Thus, the amplitude of the sidebands is directly proportional to the modulator amplitude and inversely proportional to the offset frequency. These relationships can be transferred into the dB power domain:

$$SidebandPower[dBm] = k \cdot 20 \cdot \log\left(\frac{\Delta\omega}{\omega_o - \omega_i}\right) \quad (4.5)$$

where  $k$  represents the proportionality constant.

Some of the measurements presented on section 4.3 can be justified from (4.3), (4.4), (4.5) and Fig.4.18. The sidebands shown in 4.7 are caused by the frequency modulation of the LC-VCO output signal due to the pulling effect caused by the HFSN. The amplitude of both sidebands is the same because of being a narrow-band frequency modulation and they have a frequency offset equal to the modulation frequency, which, under pulling effect, is equal to the subtraction between the free oscillation frequency,  $\omega_o$ , and the HFSN frequency,  $\omega_i$ . The 20 dB/dec sideband amplitude relationship with the offset frequency is caused by the inverse proportionality between the sideband amplitude and

the modulation frequency, shown in (4.5). The behavior of the  $\omega_i$  sideband when the frequency offset is very small is caused by the strong pulling effect shown in Fig.4.16-b which breaks the  $20\text{ dB/dec}$  relationship. For very high frequency offsets, the  $\omega_i$  sideband reaches a minimum stable level due to the direct coupling of the HFSN signal to the output buffers.

The relationship between the oscillation and HFSN amplitudes and the relative and absolute amplitudes shown in Fig.4.11 and Fig.4.13 can also be analyzed from an ILO point of view. The time domain equation 4.3 suggests that the amplitude of both the carrier and the sidebands should be increased when the amplitude of the LC-VCO increases as the term  $A_o$  is a multiplying factor to the whole oscillator term of (4.3). This results seems to contradict the conclusions from the measurements shown in Fig.4.13. Chapter 5 will show that the multiplier factor is compensated by the characteristics of the frequency modulation. This effect will be analyzed and justified in detail in Chapter 5. Regarding the effect of the HFSN amplitude,  $A_i$ , equations (4.4) and (4.5) show the proportionality between the sideband amplitude and the frequency deviation,  $\Delta\omega$  and, consequently, the proportionality between the sideband amplitude and the HFSN amplitude, justifying the measurements presented in Fig.4.11.

Finally, the NBFM approach can also explain the occupied bandwidth of each of the sidebands. The measurement of the occupied bandwidth was shown in Fig.4.12. The modulation frequency is equal to the frequency offset,  $\omega_o - \omega_i$ . As it has already been commented, the injected tone has a very small occupied bandwidth due to the high quality of the laboratory equipment and can be considered as a pure tone at a fixed frequency,  $\omega_i$ . The free oscillation frequency of the LC-VCO is affected by several mechanisms that randomly modify the instantaneous oscillation frequency. The output spectrum of the LC-VCO shows an occupied bandwidth around the center oscillation frequency due to the frequency deviation. In the particular case shown in Fig.4.12, the occupied bandwidth of the LC-VCO is around 1 MHz. Consequently, the offset frequency,  $\omega_o - \omega_i$ , and so, both the modulation frequency and the sideband at  $2\omega_o - \omega_i$ , are also affected by the deviation of  $\omega_o$ . Thus, the instantaneous oscillation frequency of the LC-VCO determines the instantaneous modulation frequency. Fig.4.19 shows a diagram with the two extreme cases (maximum and minimum  $\omega_o$ ) which graphically explains the reason why the sideband at  $2\omega_o - \omega_i$  has the double occupied bandwidth than the LC-VCO.

From a mathematical point of view, the LC-VCO oscillation frequency can be formulated as:

$$\omega_o \pm \Delta\omega_o/2 \quad (4.6)$$

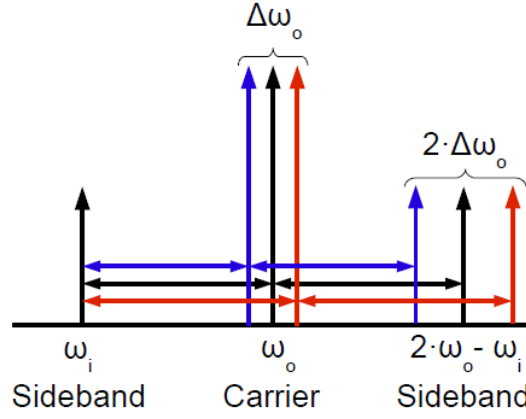


Figure 4.19. Diagram of the mirror sideband generation for the maximum and minimum LC-VCO oscillation frequencies

where  $\Delta\omega_o$  represents the frequency deviation and is, therefore, half of the occupied bandwidth.

Once the HFSN is injected, one sideband will appear at  $\omega_i$  and another one at the mirror frequency opposite to the HFSN. So, mathematically the opposite frequency,  $\omega_{op}$  :

$$OpositeFrequency = OscillationFrequency - FrequencyOffset \quad (4.7)$$

$$\omega_{op} = \omega_o \pm \Delta\omega_o/2 - [\omega_i - (\omega_o \pm \Delta\omega_o/2)] \quad (4.8)$$

$$\omega_{op} = (2\omega_o - \omega_i) \mp \Delta\omega_o \quad (4.9)$$

According then to equation 4.9 the sideband generated at the mirror frequency has a center frequency  $2\omega_o - \omega_i$  and an occupied bandwidth  $2\Delta\omega_o$ . This conclusion perfectly fits the measurement shown in Fig.4.12.

## 4.5 Summary and conclusions

This chapter has empirically analyzed the effect of HFSN on a particular LC-VCO with objective to find how the oscillator performance is degraded and which parameters have a relevant role in the robustness of the oscillator to the HFSN. This experiment emulates the scenario where an LC-VCO (victim) is perturbed by another high power RF system (aggressor), like a power amplifier. The manufactured chip contains a  $7\text{ GHz}$  LC-VCO where it is possible to inject noise into the substrate using a pad. The first observation shows that a high frequency tone with a frequency similar to

that of the LC-VCO injected in the substrate generates two sidebands in the output spectrum of the LC-VCO. One sideband at the same frequency of the injected noise,  $\omega_i$ , and the other one at the mirror frequency,  $2\omega_o - \omega_i$  (same frequency offset but at the opposite side. Several tests have been carried out to show the main correlation between the degradation of the oscillator output and the main characteristics of both, oscillator and noise. Two candidates have been proposed as the main interaction mechanisms between the HFSN and the LC VCO: intermodulation between the HFSN and the oscillator at the oscillator tank and frequency pulling of the oscillator due to the HFSN.

The results of the measurements have been analyzed with the objective of answering the following question: Can intermodulation or pulling fully explain the measured effects of HFSN on the LC-VCO? The empirical analysis has shown that the answer to this question is that the pulling effect of the HFSN on the LC-VCO is the main cause of the LC-VCO performance degradation. The HFSN perturbed LC-VCO behaves like an ILO that has lost the synchronization with the injected signal. The output of the oscillator is modulated in frequency by the noise due to the pulling effect of the HFSN. In the analyzed case, where the noise is a pure frequency tone, the output of the perturbed oscillator can be modeled using a narrow band frequency modulated signal. All the relationships found through measurements between the degraded output spectrum and the HFSN and oscillator characteristics, except one (sideband amplitude vs oscillator amplitude) can be justified using the pulling effect as the interaction mechanism.

The empirical analysis concludes that a noise tone with a frequency similar to the free running oscillator frequency injected in the substrate can travel through it and reach the LC-VCO and, due to pulling effect, it can modify the instantaneous phase of the oscillation and, consequently, degrade the LC-VCO output signal. A deep and detailed mathematical analysis of the interaction between the oscillator and the HFSN is necessary with the objective of finding the characteristics and properties of the LC-VCO or of the HFSN that can increase the robustness of the oscillator to HFSN.

## Chapter 5

# Modeling the effect of HFSN on LC-VCOs.

### 5.1 Introduction and objectives

The measurements and the analysis performed on the LC-VCO presented in chapter 4 have identified injection pulling as the main cause of the oscillator performance degradation due to HFSN. This chapter introduces the effect of pulling on LC-VCOs from a more theoretical point of view. The theory of injection locked oscillators is presented and used to discuss and validate the conclusions obtained in chapter 4. The main objective of this chapter is to show that, thanks to the simplification of the injection locked oscillator theory in our particular scenario, it is possible to create a model that can predict the behavior of an LC-VCO under the interference of HFSN. This simple model will be very useful to easily predict the effect of HFSN on LC-VCOs as well as to obtain insight for the design of HFSN robust LC-VCOs.

This chapter firstly presents a description of the frequency pulling and locking effects. After that, the LC-VCOs and the frequency pulling and locking effects are analyzed from a mathematical point of view, with special interest in the scenario where these effects are caused by HFSN. The conclusions of this analysis will lead to a simple model that predicts the behavior of an LC-VCO perturbed by HFSN. This model will be compared against the measurements presented in chapter 4 to evaluate the qualitative accuracy of the model. Finally, a simulation test bench, created to simulate the effect of HFSN on an ideal LC-VCO, allows to analyze the quantitative accuracy of the model.

## 5.2 Pulling and locking effects in oscillators

### 5.2.1 Definition of the frequency pulling and locking effects

Frequency pulling and frequency locking are effects that can alter the oscillation frequency of a harmonic oscillator, caused by the perturbation of an external entity, usually of oscillatory nature too, like a second oscillator or a periodical change in the surrounding environment. Frequency pulling is usually referred when the external perturbation can only slightly and temporally modify the oscillation frequency of the oscillator. When this perturbation is very strong the oscillator can completely and permanently change its frequency to replicate the frequency of the perturbation, locking the oscillator. This is called frequency locking. Although frequency pulling and locking are very commonly unwanted effects that can threaten the proper performance of an oscillator, several positive and beneficial effects have been found with their usage. Frequency pulling and frequency locking effects are natural processes of every oscillator, electrical, mechanical and even biological. There are a lot of "oscillators" in biological processes that can show pulling and locking effects. The most famous oscillator in biology is the heart. It is well known that a heart can be forced to beat at a particular frequency using electrical stimulation or a pacemaker [93]. Beneficial effects to mitigate the effects of diseases like epilepsy or Parkinson have been accomplished with the electrical modulation of the nervous system using periodical pulses [94], [95]. Other biological systems also present the effect of pulling and locking: tidal rhythm modify the natural rhythm of several beings, for example, the oxygen consumption and the color of fiddler crabs can be controlled with artificial tidal generation [96], [97], and there are video recordings [98] showing the synchronous blink of fireflies in the Great Smoky Mountains. Mechanical oscillators also show these effects. Actually, one of the earliest references to the interaction and synchronization of oscillators, back in the 17th century [99], comes from the Dutch scientist Christiaan Huygens, who realized that the pendulums of the clocks hung in the same wall oscillate synchronously. He even foresaw that the synchronization was due to the vibrations through wall. The expressions pulling and locking are more commonly used in electronics. Frequency pulling and locking in electronic circuits are, in some cases, harmful and negative effect. Several examples of the interaction between electronic circuits have been already commented in the previous chapters, such as the harmful interaction between the power amplifier (PA) and the LC-VCO [50] in an RF transceiver which can modify the oscillation frequency of the LC-VCO. The sensitivity of the RF transceiver can also be easily overwhelmed by the effect of the high frequency

substrate noise (HFSN) caused by the high frequency harmonics of a digital clock [10]. But, as in the case of biological oscillators, several useful applications of the frequency pulling and locking have been reported, like frequency synthesizing with Phase Locked Loops (PLL) [100], [101] or frequency dividers [102], [103] and frequency quadrature generation [104]. Several communication systems make use of the frequency pulling or locking, like frequency demodulators [105] or carrier recovery when a suppressed carrier modulation scheme is used [106]. In order to fully define the effect of frequency pulling and locking in oscillators it is necessary to dive into the basic mathematics of oscillators.

### 5.2.2 Mathematical introduction to LC-VCOs

Any LC oscillator can be modeled as a tank, where the actual oscillation takes place, and an active inverting feedback stage, where the amplification takes place, as shown in Fig.5.1. The tank is build with the parallel combination of an inductor and a capacitor, creating a frequency selective impedance that allows the oscillation to take place at a particular frequency. The active part of the oscillator is responsible to compensate the loss in the tank through amplification. It is usually modeled as a negative resistance that injects energy in the tank in a particular way to create the stable oscillation. In order to obtain a continuous over time oscillation two requirements should be granted.

- the negative impedance of the active network should cancel out the losses of the tank.
- the closed loop gain should have a total zero phase shift.

These two conditions lead to a closed loop gain with a magnitude larger than the unity and purely real (no imaginary component).

A real implementation example of an LC oscillator is shown in Fig.5.2. In this case, the tank is modeled using a parallel combination of an inductor, a capacitor and a resistor, which accounts for the losses of the tank. The two transistors, thanks to the cross coupled scheme connection, provide the required amplification and phase shift to grant the oscillation.

The oscillator works as follows:

- The tank works as a 1-port device with an input impedance  $Z(s)$ . The impedance of the tank converts the current flowing through it into voltage. The voltage at node  $V_{outA}$  decreases when the current crossing the tank increases due to  $V_{outA} = V_{DD} - V_{tank}$ . From a phase point of

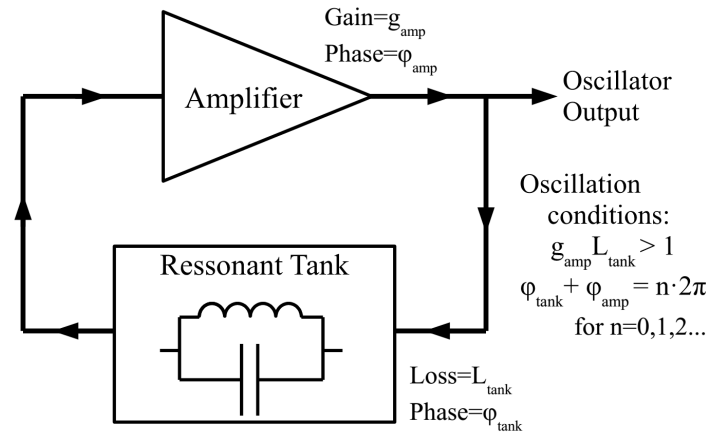


Figure 5.1. Block diagram of a resonant based oscillator

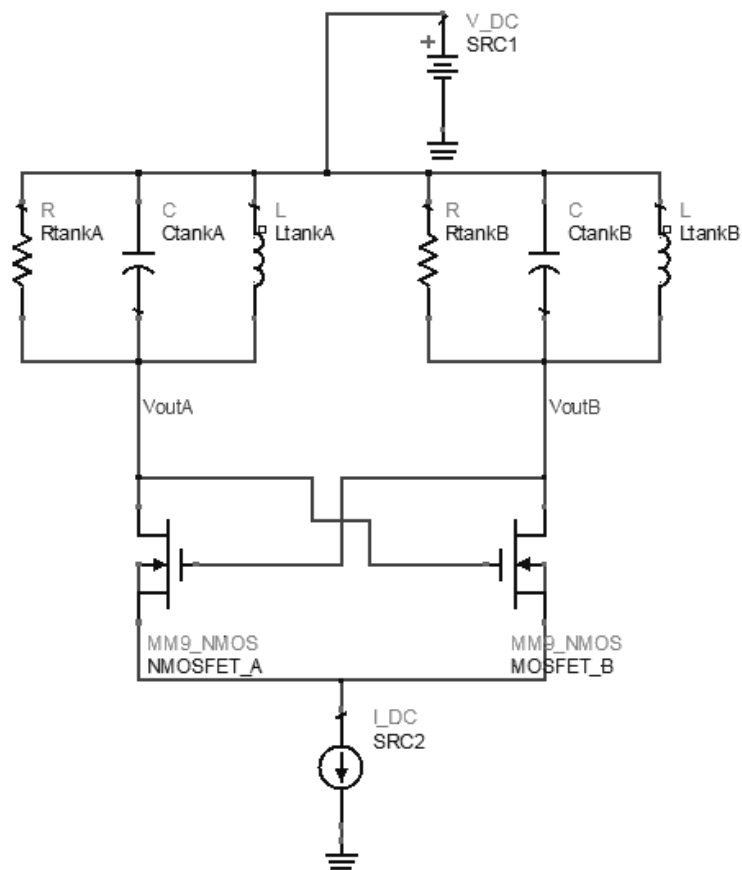


Figure 5.2. Schematic of a typical NMOS LC oscillator

view, there is a phase shift of  $180^\circ$  between  $V_{outA}$  and the current, but only at the resonance frequency



- The two mosfets have their gate terminals connected to the opposed branch. If the voltage on the gate rises, the current between its source and drain terminals increases, increasing also the tank voltage drop. The NMOS transistors provide the required energy to compensate the losses of the tank through its trans-conductance gain ( $g_m$ ). On the other hand, the cross coupled connection provides the required  $180^\circ$  to accomplish with the necessary total zero phase shift.

Under these conditions, oscillation is possible at the resonance frequency of the tank.

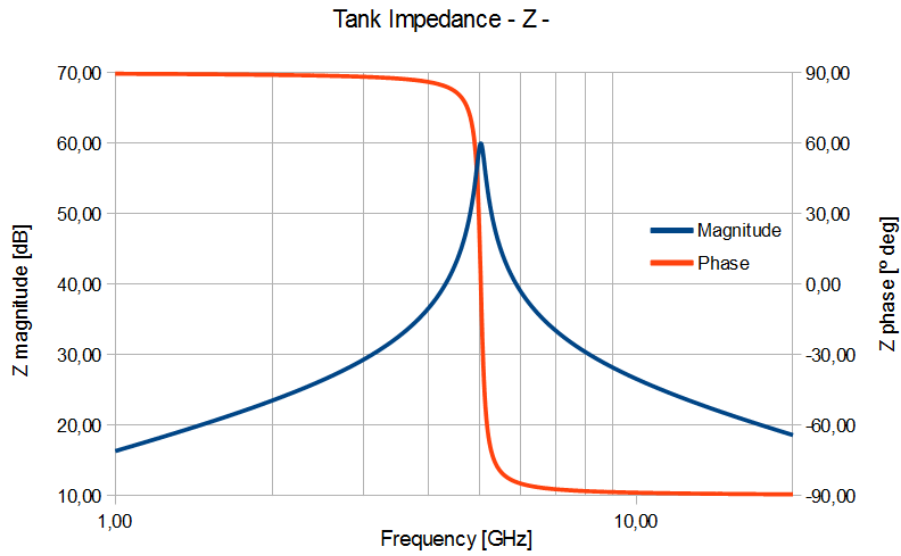


Figure 5.3. Magnitude and phase of the tank impedance.

The analysis of the oscillator starts with the tank admittance, which, for the parallel resonance tank presented in Fig.5.2 is:

$$Y(s) = \frac{1}{R} + \frac{1}{sL} + sC \quad (5.1)$$

$$Y(s) = \frac{s^2RLC + sL + R}{sRL} \quad (5.2)$$

The magnitude and phase of a typical resonant tank is shown in Fig.5.3.

The resonance frequency of the parallel tank is the frequency where the admittance is pure real.

Using  $s = jw$  and  $imag(Y(s)) = 0$ :

$$imag(Y(s)) = \frac{R - \omega^2RLC}{\omega RL} = 0 \quad (5.3)$$

and, so, the resonance frequency,  $\omega_o$  is:

$$\omega_o = \frac{1}{\sqrt{LC}} \quad (5.4)$$

Another important physical parameter of the oscillator tank is the quality factor (Q). The quality factor is a key parameter of the tank that has a huge influence on the performance of the oscillator in terms of oscillation amplitude, spectral purity and phase noise. Q can actually be thought as a figure of merit that quantifies how close is a real oscillator to an ideal lossless oscillator. Three different definitions for Q can be found [107], [108]:

- From an energy point of view: Ratio between the energy stored and the energy dissipated per cycle .

$$Q = 2\pi \frac{\text{energyStored}}{\text{energyDissipated}} \quad (5.5)$$

- From a bandwidth point of view: ratio between the resonance frequency and the half power bandwidth, as shown in 5.4

$$Q = \frac{\omega_o}{\text{BandWidth}} \quad (5.6)$$

- From a phase point of view: product of the frequency and the slope of the phase of the open-loop transfer function at the resonance frequency of the tank.

$$Q = \frac{\omega_o}{2} \left| \frac{d\phi(\omega)}{d\omega} \right|_{\omega=\omega_o} \quad (5.7)$$

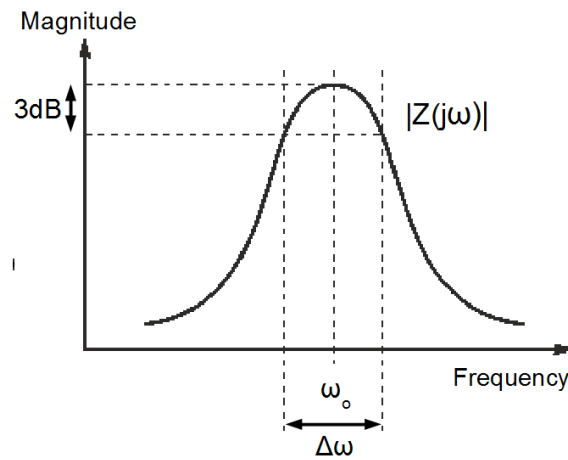


Figure 5.4. Definition of quality factor from a bandwidth point of view

The quality factor can be related to the tank RLC parameters using the tank admittance (5.2) and (5.7). The phase of the tank is defined as:

$$\phi(j\omega) = \tan^{-1} \left( \frac{\text{Imag}(Y(j\omega))}{\text{Real}(Y(j\omega))} \right) \quad (5.8)$$

$$\phi(j\omega) = \tan^{-1} \left( \frac{R(1 - \omega^2 LC)}{\omega L} \right) \quad (5.9)$$

so, using (5.7)

$$\frac{d\phi}{d\omega} = \frac{1}{1 + \left( \frac{R}{\omega L} (1 - \omega^2 LC) \right)^2} \left[ \frac{R}{\omega^2 L^2} (1 - \omega^2 LC) - 2CR \right] \quad (5.10)$$

Taking into account (5.4), and that  $(1 - \omega_o^2 LC) = 0$ , then:

$$\left. \frac{d\phi}{d\omega} \right|_{\omega=\omega_o} = -2CR \quad (5.11)$$

So,

$$\frac{\omega_o}{2} \left| \frac{d\phi}{d\omega} \right|_{\omega=\omega_o} = \omega_o CR \quad (5.12)$$

At the resonance frequency the magnitude of the inductor admittance  $|Y_L| = 1/\omega_o L$  is equal to the magnitude of the capacitor admittance  $|Y_C| = \omega_o C$ , then, the quality factor of a parallel RLC resonance tank can be defined as:

$$Q = \frac{\omega_o}{2} \left| \frac{d\phi}{d\omega} \right|_{\omega=\omega_o} = \omega_o CR = \frac{R}{\omega_o L} \quad (5.13)$$

The presented definitions of  $\omega_o$  and  $Q$  will help in the mathematical analysis of the pulling effect.

### 5.2.3 Mathematical analysis of the pulling effect on LC-VCOs

It has already been empirically shown that an external signal that reaches the tank can modify the output spectrum of the oscillator. A mathematical analysis of this situation can be performed following the analysis presented in section 5.2.2. Adler [89] presented a mathematical method in order to obtain a behavioral model to describe ILOs. This method is also followed in this work.

The following analysis, based on Adler analysis, assumes an oscillator working at its natural frequency  $\omega_o$  with an amplitude  $A_o$  perturbed by a pure tone at a frequency  $\omega_i$  and an amplitude  $A_i$ . Note that due to the passive nature of the resonant tank,  $A_o$  and  $A_i$  can be indifferently considered in both the voltage or current domain, and so,

$$\frac{A_i}{A_o} = \frac{V_i}{V_o} = \frac{I_i}{I_o} \quad (5.14)$$

Two further restrictions are assumed:

- The injected frequency is close to the free running oscillator frequency. More precisely, the injected frequency lays far within the bandpass of the oscillator. So,

$$2\Delta\omega_o \ll \text{Bandwidth} \quad (5.15)$$

where  $\Delta\omega_o = \omega_o - \omega_i$ . Consequently, using (5.6)

$$\frac{\omega_o}{2\Delta\omega_o} \gg \frac{\omega_o}{\text{BandWidth}} \Rightarrow \frac{\omega_o}{\Delta\omega_o} \gg 2Q \quad (5.16)$$

- The oscillation amplitude is much bigger than the injected tone amplitude. So,

$$A_o \gg A_i \Rightarrow \frac{A_i}{A_o} \ll 1 \quad (5.17)$$

The instant voltage in the oscillator tank can be represented using a phasor diagram. Fig.5.5 shows the phasor representation of both, the oscillator and the injected signal, referenced to the injected signal frequency. This means that any signal at a frequency  $\omega_i$  will be represented as an steady (not rotating) vector. The size of the vector and its angle represent the amplitude and the phase of the oscillation respectively. Consequently, a signal with a frequency different from  $\omega_i$  will rotate due to the changing phase difference with the reference signal. Thus, the angular speed of rotation is determined by difference between the oscillation frequency and the injected frequency. The two voltages are added by superposition, resulting in an output vector with magnitude  $A_p$  which has been phase shifted by an angle of  $\phi$  from the free running original oscillation phase. The rate of change of the phase shift determines the output frequency of the system as following:

$$\omega - \omega_i = \frac{d\alpha}{dt} \quad (5.18)$$

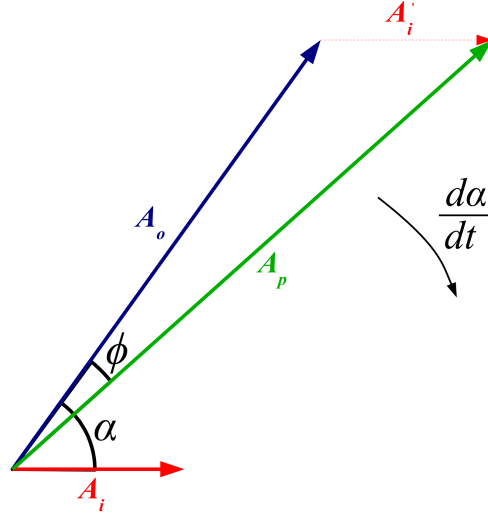


Figure 5.5. Phasor representation of the oscillator signal

One can see that the shift angle  $\phi$  can be related to the phase difference between the oscillator and injected signals,  $\alpha$ . Using the trigonometric Law of Sine [109]:

$$\frac{A_i}{\sin \phi} = \frac{A_p}{\sin (\pi - \alpha)} \quad (5.19)$$

Taking into account the condition  $A_o \gg A_i$ , presented at (5.17), the magnitude of  $A_o$  and  $A_p$  are necessarily almost equal. So:

$$\frac{A_i}{-\sin \phi} = \frac{A_o}{\sin (-\alpha)} \quad (5.20)$$

The second of the conditions just presented, (5.17) implies that  $\phi$  is a very small angle, allowing further simplification.

$$\phi \approx = \frac{A_i}{A_o} \sin \alpha \quad (5.21)$$

It is very important to note the phase shift created by the injected signal breaks the oscillation condition presented in section 5.2.2. If nothing else changes, the total phase shift of the oscillator is not longer  $360^\circ$ , due to the phase shift added by the injected signal. Something needs to change in the tank in order to compensate the phase shift added by the injected signal. The relationship between the phase shift of the tank and the frequency was already presented in Fig.5.3. A zoom of Fig.5.3 around the tank resonance frequency is shown in Fig.5.6. It shows that at the resonance frequency,

$\omega_o$ , the tank generates a  $0^\circ$  phase shift, which translates in a  $180^\circ$  phase shift of  $V_{out}$ . If the injected signal adds a phase shift (positive or negative) the tank phase shift should be different than  $0^\circ$ . This is what happens, for example, at  $\omega_{ph}$ , where the phase shift is  $30^\circ$ . So, in this example, if the injected signal is causing a  $30^\circ$ ,  $V_{out}$  should be phase shifted by  $-30^\circ$ , which corresponds to a  $30^\circ$  phase shift of the tank impedance. Consequently, the tank compensates the phase shift of the oscillation signal by slightly changing the oscillation frequency. In the example, the oscillation frequency changes to around  $4.98\text{ GHz}$ . Due to the assumption presented at (5.16), the phase shift will be very small and it will lay within the bandwidth of the tank. In that region the phase of the tank can be approximated by a straight line which slope will be given by the first derivative of the phase with respect to the frequency.

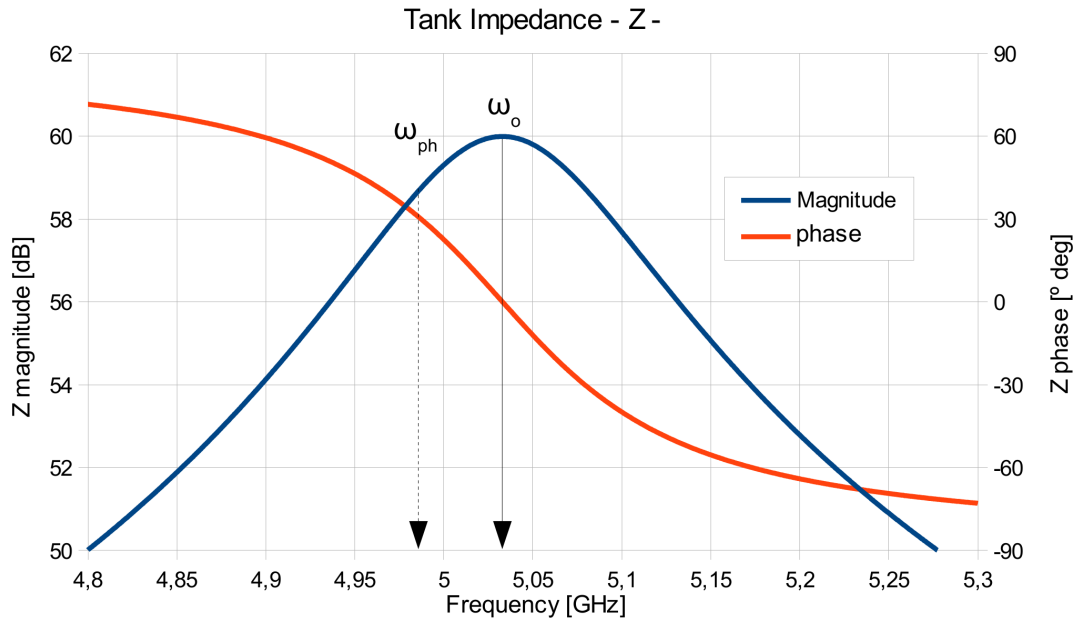


Figure 5.6. Example of the frequency change in the tank caused by the phase shift.

$$M = \frac{d\phi}{d\omega} \quad (5.22)$$

And so, the phase shift caused by a frequency  $\omega$  around  $\omega_o$  will be given by:

$$\phi = M(\omega - \omega_o) = M((\omega - \omega_i) - (\omega_o - \omega_i)) = M\left(\frac{d\alpha}{dt} - \Delta\omega_o\right) \quad (5.23)$$

This equation can be solved more easily if the phase of the tank is expressed in terms of  $Q$  and  $\omega_o$ . Starting from (5.9):

$$\tan \phi = \frac{(1 - \omega^2 LC) R}{\omega L} \quad (5.24)$$

Using the already presented definition of  $Q$  and  $\omega_o$  on (5.13) and (5.4):

$$\tan \phi = \left(1 - \frac{\omega^2}{\omega_o^2}\right) \frac{R}{\omega L} = \left(1 - \frac{\omega^2}{\omega_o^2}\right) \frac{Q \omega_o}{\omega} = \frac{(\omega_o^2 - \omega^2) Q}{\omega \omega_o} \quad (5.25)$$

Since  $(\omega_o^2 - \omega^2) \approx 2\omega(\omega_o - \omega)$ , then,

$$\tan \phi = \frac{2Q(\omega_o - \omega)}{\omega_o} \quad (5.26)$$

For values of  $\omega$  close to  $\omega_o$  the value of  $\tan \phi$  is very small and, so, the approximation  $\tan^{-1}(x) \approx x$ . The slope can be finally obtained.

$$M = \frac{d\phi}{d\omega} = \frac{d}{d\omega} \left( \tan^{-1} \left( \frac{2Q(\omega_o - \omega)}{\omega_o} \right) \right) = \frac{d}{d\omega} \left( \frac{2Q(\omega_o - \omega)}{\omega_o} \right) = -\frac{2Q}{\omega_o} \quad (5.27)$$

Starting with equation (5.23):

$$\phi = M \left( \frac{d\alpha}{dt} - \Delta\omega_o \right) \quad (5.28)$$

And combining it with (5.21) and (5.27):

$$\frac{A_i}{A_o} \sin \alpha = -\frac{2Q}{\omega_o} \left[ \frac{d\alpha}{dt} - \Delta\omega_o \right] \quad (5.29)$$

And, so, concluding:

$$\frac{d\alpha}{dt} = -\frac{A_i \omega_o}{A_o 2Q} \sin \alpha + \Delta\omega_o \quad (5.30)$$

### 5.3 Modeling HFSN effect on LC-VCO

The presented analysis has concluded with a model, (5.30), which can accurately predict the behavior of an ILO both under locking and under pulling. This model has been the starting milestone of several studies that have tried to extract simpler or analytical expressions that can be easily used to calculate particular parameters of the ILO or VCO. One of the first detailed and relevant analysis was done by H.L.Stover back in 1966 [90]. Stover provided a closed expression to calculate some important parameters, like the frequency shift and the output sidebands frequencies, of an ILO that is very close to lock and so, under a very strong pulling effect. He used a polynomial approximation of the phase to solve Adler's differential equation (5.30). M.Armand [91] and J.Deckleva [110] presented, a few years after Stover's work, a similar study based on an expansion of the phase in Fourier series. B.Biswas [111] also presented a very detailed analysis of the effect of the amplitude modulation on locking range and the amplitude limiting effect of the tank. More recently, the studies are mainly oriented to exploit the today's high computational power to numerically simulate the behavior of the ILO and the VCO. For example, X.Lai [112] presents a macromodel that can be used to accurately and efficiently simulate the behavior of the oscillator under locking and pulling, being able to predict, for example, the output spectrum and the dynamics of the transition to locking, including unlocked tones and phase jumps.

The results, in the form of behavioral or analytical models, mathematical expressions, etc, are a huge source of solutions to analyze the effect of a signal injected into an oscillator. They can very accurately predict the behavior of the injection locked oscillator both in the locked and in the unlocked regions. The main problem of all of them is that they are mainly focused in the case where the oscillator is very close to lock (actually, the main case of interest when working with ILO) resulting in complex, and hardly intuitive, expressions. All these expressions are also rarely specifically stated for LC-VCO and so, they are usually not related to the LC-VCO parameters. The analysis of the effect of HFSN on LC-VCOs can be further enclosed compared to the scenario presented in those previous works. The amplitude of the noise reaching the oscillator after traveling through the substrate is generally very small compared to the oscillation amplitude. In this case, it has been shown in chapter 4 that the HFSN can pull the oscillator but very weakly. Only when the injected signal is very close to the oscillation frequency or when it is extremely powerful (probably far beyond the power that a real device can inject into the substrate) and directly injected (direct connection) into the substrate, the oscillator shows the effect of strong pulling or locking. The inclusion of this



condition into the conclusion of the previous analysis (5.30) provides a closed and intuitive model that relates the robustness of the LC-VCO to HFSN with the design parameters of the LC-VCO.

The time domain behavior of an oscillator under pulling or locking can be mathematically expressed using the following equation.

$$v(t) = A(t) \sin [\omega_i t + \alpha(t)] \quad (5.31)$$

where  $\omega_i$  is the frequency of the noise injected signal,  $A(t)$  is the output amplitude, and  $\alpha(t)$  is the differential phase between the injected signal and the VCO output. The phase difference between both signals is described by the already presented differential equation (5.30) :

$$\frac{d}{dt} \alpha(t) = -\frac{A_i}{A_o} \frac{\omega_o}{2Q} \sin[\alpha(t)] + (\omega_o - \omega_i) \quad (5.32)$$

Under locking,  $\omega_o = \omega_i$  and, so, the phase of (5.31) is constant. Consequently:

$$\frac{d}{dt} \alpha(t) = 0 \quad (5.33)$$

$$\sin[\alpha(t)] = \frac{2Q}{\omega_o} \frac{A_o}{A_i} (\omega_o - \omega_i) \quad (5.34)$$

Taking into account that  $\sin[\alpha(t)]$  is limited to the range  $\pm 1$ , then, (5.34) can only be solved if:

$$\left| \frac{\omega_o}{2Q} \frac{A_i}{A_o} \right| < (\omega_o - \omega_i) \quad (5.35)$$

The physical interpretation of (5.35) shows that locking is only possible if the frequency offset,  $\omega_o - \omega_i$ , lays within a limited frequency range. This frequency range is determined by the injected amplitude  $A_i$ , the oscillation frequency  $\omega_o$  and amplitude  $A_o$  and the tank quality factor  $Q$ . When the power of the injected signal is very high or the frequency offset is very small, the LC-VCO locks to the noise signal and is forced to oscillate at the injected frequency,  $\omega_i$ .

$$LockingRange = B = \frac{\omega_o}{2Q} \frac{A_i}{A_o} \quad (5.36)$$

This definition of the locking range justifies the proposed scenario where the HFSN is only causing weak pulling on the LC-VCO. In this scenario, the amplitude of the HFSN reaching the

tank,  $A_i$  is several orders of magnitude smaller than the oscillation amplitude  $A_o$ , consequently, the locking range is several orders of magnitude smaller than the oscillation frequency  $\omega_o$ . Strong pulling or locking would be only possible when the frequency offset is extremely small. So, in the case where the noise couples into the tank through the substrate, the noise signal reaching the tank is typically very weak compared with the oscillation amplitude and cannot get the oscillator to lock, but it is enough to perturb its phase. The effect of the noise tone in the phase of the oscillator depends on the difference between their phases. Given that the noise and the oscillator have different frequencies, the phase difference varies with time and, consequently, the instantaneous frequency of the oscillator is modified. The conclusions of the empirical analysis of the effect of HFSN on an LC-VCO presented in chapter 4 suggest that the output of the oscillator is frequency modulated by the HFSN.

With the objective of finding a simple and intuitive model valid for the analysis of HFSN effects on LC-VCOs, the following solution for (5.32) is proposed based on the assumption that the sidebands presented in chapter 4 are caused by a narrowband FM modulation of the LC-VCO output.

$$\alpha(t) = (\omega_o - \omega_i)t + \frac{B}{(\omega_o - \omega_i)} \cos[(\omega_o - \omega_i)t] \quad (5.37)$$

where B is equal to the locking range defined in (5.36).

Substituting the proposed solution (5.37) on both sides of (5.32) the following results are obtained. Left hand side of (5.32):

$$\frac{d}{dt}\alpha(t) = (\omega_o - \omega_i) - B \sin[(\omega_o - \omega_i)t] \quad (5.38)$$

Right hand side of (5.32):

$$-B \sin[\alpha(t)] + (\omega_o - \omega_i) = (\omega_o - \omega_i) - B \sin[(\omega_o - \omega_i)t + \frac{B}{(\omega_o - \omega_i)} \cos[(\omega_o - \omega_i)t]] \quad (5.39)$$

Which can be rewritten as:

$$-B \sin[\alpha(t)] + (\omega_o - \omega_i) = (\omega_o - \omega_i) - B \sin[(\omega_o - \omega_i)t + \xi] \quad (5.40)$$

where  $\xi$  represents the error that differentiates both sides of solved equation.

$$\xi = \frac{B}{(\omega_o - \omega_i)} \cos[(\omega_o - \omega_i)t] \quad (5.41)$$

The comparison between the left and the right hand sides terms shows that the proposed solution (5.37) can only be valid if the error  $\xi$  is no relevant. Analyzing (5.41), the error term  $\xi$  is limited:

$$\xi < \frac{B}{(\omega_o - \omega_i)} [\text{radians}] \quad (5.42)$$

and so, the error will be negligible when the frequency of the HFSN is far from the locking range. This condition is perfectly aligned with the presented scenario and so, the proposed solution, (5.37), can be considered as a solid candidate to analyze the effect of the HFSN on LC-VCOs.

The obtained modeled time domain behavior of the LC-VCO under the effect of HFSN, shown in (5.43), is obtained putting together (5.31) and (5.37),

$$v(t) \simeq A_o \sin \left[ \omega_o t - \frac{A_i}{A_o} \frac{\omega_o}{2Q(\omega_o - \omega_i)} \cos [(\omega_o - \omega_i)t] \right] \quad (5.43)$$

which corresponds to a frequency modulated signal with a maximum frequency deviation of:

$$\text{frequency Deviation} = \frac{\omega_o}{2Q} \frac{A_i}{A_o} \quad (5.44)$$

and a frequency offset of:

$$\text{frequency Offset} = (\omega_o - \omega_i) \quad (5.45)$$

One final step should be taken to obtain the predicted output spectrum of the perturbed LC-VCO. As it has been already commented, the solution presented in (5.43) can be analyzed as a carrier modulated by a sine signal. The Bessel function of the first kind,  $J_n(x)$ , can be used to approximate (5.43) by a summation of sine signals at frequencies  $\omega_o \pm n(\omega_o - \omega_i)$  [113]. Consequently, the amplitude of the carrier and of all the spectrum sidebands can be obtained through the following analysis:

$$CarrierAmplitude = A_o \cdot J_0 \left( \frac{A_i}{A_o} \frac{\omega_o}{2Q(\omega_o - \omega_i)} \right) \quad (5.46)$$

$$nSidebandAmplitude = A_o \cdot J_n \left( \frac{A_i}{A_o} \frac{\omega_o}{2Q(\omega_o - \omega_i)} \right) \quad (5.47)$$

In the presented scenario, it has been shown that, firstly, the oscillation amplitude is much higher than the amplitude of the noise reaching the tank and, secondly, the offset between the oscillation frequency and the noise frequency cannot be too small compared with the oscillation frequency, as then, it would fall into the locking range. The consequence of these two conditions is then:

$$\frac{A_i}{A_o} \frac{\omega_o}{2Q(\omega_o - \omega_i)} \ll 1 \quad (5.48)$$

The Bessel function of the first kind for the first five orders between  $x = 0$  and  $x = 10$  is shown in Fig.5.7. For very small values of  $x$  all the Bessel functions can be accurately approximated by linear functions, as shown in (5.51).

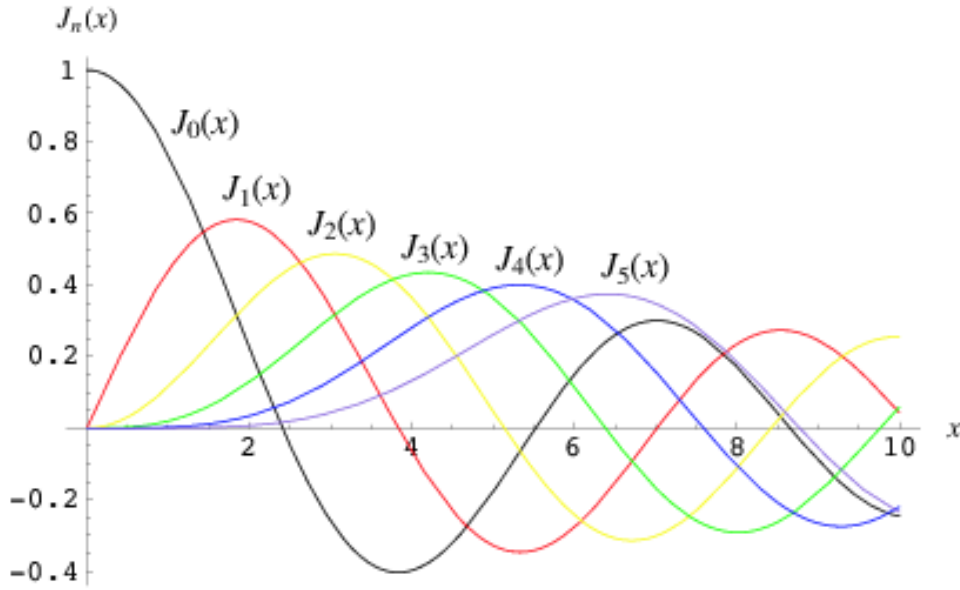


Figure 5.7. Bessel function of the first kind for the first five orders

$$J_0(x) \simeq 1 \quad (5.49)$$

$$J_1(x) \simeq 0.5 \cdot x \quad (5.50)$$

$$J_{n>1}(x) \simeq 0$$

Consequently, the amplitude of the sidebands caused by HFSN on an LC-VCO can be formulated as:

$$CarrierAmplitude \simeq A_o \quad (5.51)$$

$$1 - SidebandAmplitude \simeq 0.5 \cdot A_o \cdot \left( \frac{A_i}{A_o} \frac{\omega_o}{2Q(\omega_o - \omega_i)} \right) \quad (5.52)$$

$$n - SidebandAmplitude \simeq 0$$

Thus, the relative amplitude (in  $dB$ ) of the first sidebands is:

$$RelativeSidebandAmplitude = 20 \cdot \log \left( 0.5 \cdot \left( \frac{A_i}{A_o} \frac{\omega_o}{2Q(\omega_o - \omega_i)} \right) \right) \quad (5.53)$$

This simple analytical model presents a more particular, intuitive, and simple solution than the general theory of unlocked ILO [49], [89] in order to analyze the effect of the high frequency substrate noise on LC-VCOs. It also presents a closed expression that provides a rapid identification of the key factors that contribute to the LC-VCO performance degradation due to HFSN, relating the degradation of the LC-VCO performance due HFSN with the key design parameters of the LC-VCO ( $A_o$ ,  $\omega_o$  and  $Q$ ) and the characteristics of the HFSN ( $A_i$  and  $\omega_i$ ). Using (5.53), a designer can easily identify the available solutions to increase the robustness of an LC-VCO to HFSN.

## 5.4 Validation of the HFSN model

The presented model needs to be validated to confirm its accuracy to predict the effect of HFSN on an LC-VCO. This section faces the validation process from two points of view. Firstly, the model will be used to analyze all the measurements presented in chapter 4. All the dependencies found back on chapter 4 will be analyzed with the model. Secondly, the model will be compared against the simulation of an LC-VCO under the effect of HFSN. The validation process will show the accuracy and the limitations of the proposed model.

### 5.4.1 Model application to measurements analysis

Back on chapter 4, several measurements were presented showing the degradation of LC-VCO output spectrum when a high frequency tone was injected in the substrate. Several parameters and

characteristics of the LC-VCO and of the tone were modified to analyze the effect on the output spectrum. Some behavioral patterns were identified thanks to those measurement. The presented model should be a useful tool to analyze the interaction between the HFSN and the LC-VCO. Those identified patterns will be individually analyzed in this section. The following dependencies were identified from the chapter 4 measurements:

- Dependence between the sideband amplitude and the frequency offset.

As the frequency offset between the oscillation frequency and the HFSN frequency increases the amplitude of the sidebands drops at a rate of  $20 \text{ dB/dec}$ . This can also be explained as an inverse proportionality between the frequency offset and the sideband amplitude. The proposed model, (5.53), correctly predicts this behavior. As a consequence, one can foresee that the RF transceiver design where the power amplifier and the local oscillator have similar frequencies, like direct conversion [114] or low-IF transceivers [115], may suffer from oscillator performance degradation due to the noise coupled through the substrate. From the model, it follows that the problem can be mitigated by separating both frequencies. One technique that exploits this approach in a real direct conversion receiver is presented in Chapter 6.

$$RelativeSidebandAmplitude = 0.5 \cdot \left( \frac{A_i}{A_o} \frac{\omega_o}{2Q(\omega_o - \omega_i)} \right)$$

- Dependence between the sideband amplitude and the amplitude of the injected HFSN.

The conclusions from Chapter 4 show that sideband amplitude and the HFSN injected amplitude have a proportional relation. This behavior is correctly modeled by (5.53). It is actually quite obvious that the less noise reaching the oscillator the less performance degradation. So, the designer should increase the isolation between the aggressor and the victim. Some techniques to increase the isolation between two areas in the substrate have already been presented and analyzed in chapter 3, concluding that protection structures, like guard rings or substrate wells, can effectively reduce the noise coupling through the substrate in some scenarios.

$$RelativeSidebandAmplitude = 0.5 \cdot \left( \frac{A_i}{A_o} \frac{\omega_o}{2Q(\omega_o - \omega_i)} \right)$$

- Dependence between the sideband relative amplitude and the LC-VCO oscillation amplitude

The only characteristic extracted from the measurements presented in chapter 4 that could not be explained with the ILO theory was the fact that the measurements in Fig.4.13 showed that the absolute sideband amplitude remained constant even if the oscillation amplitude increased, i.e. the relative sideband amplitude decreased as  $A_o$  increased. The proposed model perfectly fits the measurement results showing that the relative sideband amplitude is inversely proportional to the oscillation amplitude, as already predicted in (5.53). The interpretation of this relationship is that it is possible to increase the robustness of an LC-VCO by maximizing its oscillation amplitude. The most straight forward method to increase the oscillation amplitude is to increase the power consumption of the oscillator (until the point where the oscillation amplitude is limited by voltage instead of limited by current [116]). Some other methods to optimize the oscillation amplitude will be presented in chapter 6.

$$RelativeSidebandAmplitude = 0.5 \cdot \left( \frac{A_i}{A_o} \frac{\omega_o}{2Q(\omega_o - \omega_i)} \right)$$

Another characteristic that was detected in the measurements and analyzed in chapter 4 was the occupied bandwidth. That relationship is not addressed by the presented model as it is only oriented to obtain the amplitude of the sidebands. Anyway, the model has been obtained under the assumption that the output of the oscillator is frequency modulated by the HFSN, thus, confirming the conclusions obtained back in chapter 4 (Fig.4.19).

Finally, two more dependencies arise from the model that were not identified in chapter 4.

- Dependence between the sideband relative amplitude and the tank quality factor.

The proposed model, (5.53), shows that the quality factor of the tank has a relevant effect on the amplitude of the sidebands. The higher the tank quality factor the more robust the LC-VCO to HFSN. Consequently, it is important to maximize the quality factor of the tank in order to decrease the LC-VCO degradation due to HFSN. The effect of the tank quality factor will be deeply analyzed in chapter 7.

$$RelativeSidebandAmplitude = 0.5 \cdot \left( \frac{A_i}{A_o} \frac{\omega_o}{2Q(\omega_o - \omega_i)} \right)$$

- Dependence between the sideband relative amplitude and the oscillator frequency.

Finally, (5.53), shows that high frequency oscillators are less robust to HFSN than lower frequency ones. Usually, the oscillator frequency is not a parameter that can be chosen or modified by the designer but (5.53), together with the conclusions from chapter 3, show that special care should be taken when designing RF and mmW oscillators due to the increased sensitivity to noise and to the increased ability of HFSN to travel through the substrate at those frequencies.

$$RelativeSidebandAmplitude = 0.5 \cdot \left( \frac{A_i}{A_o} \frac{\omega_o}{2Q(\omega_o - \omega_i)} \right)$$

This section has proven the usefulness of the presented model, (5.53), to predict the behavior of an LC oscillator under the effect of HFSN from a qualitative point of view. The model has been used to justify the results obtained from the measurements performed on a real LC VCO, describing the interaction mechanisms that cause the oscillator performance degradation. The physical parameters that have a relevant effect on the oscillator robustness to the effect of HFSN have also been identified.

## 5.4.2 Analysis of the model accuracy through simulations

The previous section has validated the qualitative dependencies of the model by comparing them against the dependencies experimentally observed and reported in Chapter 5. In order to fully validate the model, a quantitative comparison would also be necessary. This is complex to do, as the model has the HFSN amplitude  $A_i$  as one of its inputs, i.e. the amount of HFSN that reached the tank, and we don't know this in the experiments. The only information available is the power of the signal injected into the substrate pad, but the amount of power that is lost between the pad and the tank is extremely difficult to determine. It would be possible to try to approximate that parameter but there are several variables in the scenario that should be taken into account, but some of them are difficult to quantify accurately. Some of these variables are:

- Return loss due to the lack of impedance adaptation in the transition RF injection probe - Substrate Pad.
- Power loss due to the transmission through the complex substrate .



- Uncertainty of the coupling paths between the substrate and the LC-VCO.
- Unpredictability of the noise distribution paths once it has reached the LC-VCO.
- Uncertainty of the return current paths from the tank back to the noise source.

Some of these items can be predicted through calculation or simulation, but some others, specially those regarding the geometrical behavior of noise currents, are extremely difficult to predict or simulate due to the complex layout of a real design. Therefore, the numerical accuracy of the presented model can not be evaluated only with the performed measurements. As an alternative method to evaluate the numerical accuracy of the presented model, (5.53), it will be compared against the simulation of an LC-VCO. A noise voltage will be superposed to the tank signal, simulating the portion of HFSN reaching the tank.

The LC-VCO is constructed with an RLC parallel tank, a cross coupled NMOS transistor pair and a common current source. The HFSN is modeled by means of two voltage sources with an offset  $180^\circ$  between them. The schematic of the LC-oscillator<sup>1</sup> is presented in Fig.5.8.

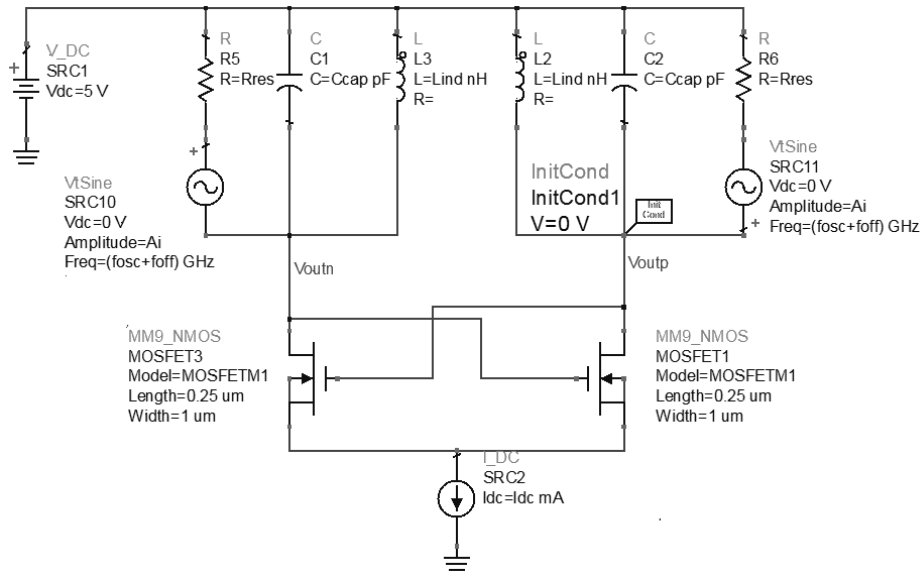


Figure 5.8. Ideal LC-oscillator with noise sources at the tank

One may ask if the noise source is correctly placed or if it should be connected in series with all the elements of the tank. Some light may be thrown into that question analyzing the system from a "current" point of view, which presents a more intuitive transition between the "real world"

<sup>1</sup>The simulated oscillator cannot actually be considered an LC-VCO due to the lack of voltage control circuitry. The obtained results are valid for both voltage controlled and non-voltage controlled oscillators.

and the model schematic. Fig.5.9 shows, according to (5.14), the same scenario than Fig.5.8. The current from the sine current source  $ItSine$  can only flow through the tank and so, the ratio  $A_i/A_o$  is equal to the injected current from  $ItSine$  divided by current flowing through the tank due to the oscillation. The transition between the current domain model and the voltage domain model can be easily obtained through Norton-Thevenin transformation, as shown in Fig.5.10.

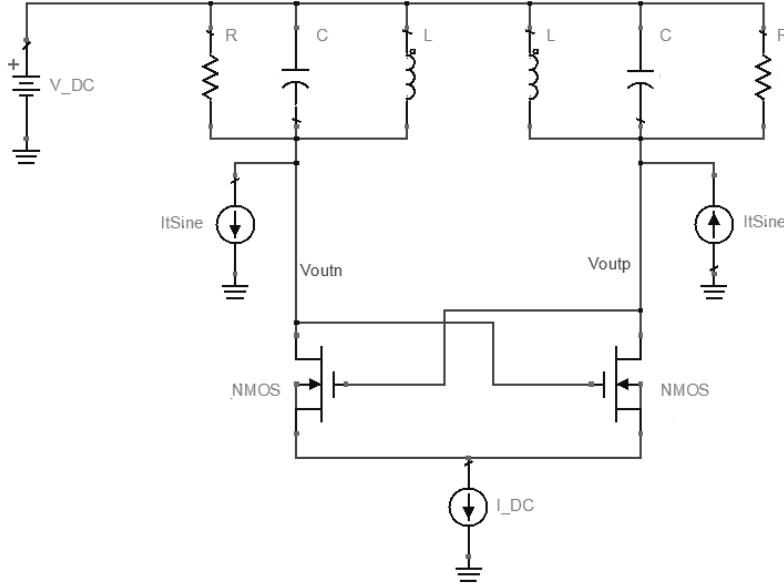


Figure 5.9. Ideal LC-VCO with current noise sources

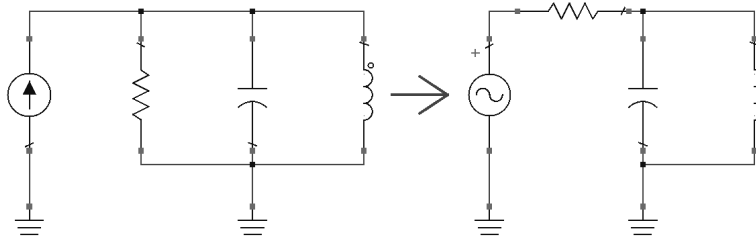


Figure 5.10. Norton and Thevenin transformation of the HFSN source.

The presented LC-VCO has been simulated using the values shown in Table 5.1. The results of the simulation show that the oscillator oscillates at a frequency of  $5.03\text{ GHz}$  with a differential amplitude of  $4.46\text{ V}_p$ . The tank quality factor can be calculated with (5.13), obtaining a value of 31.62.

The addition of the HFSN source changes the behavior of the oscillator. The noise source has an amplitude of  $10\text{ mV}$  ( $20\text{ mV}_{pp}$ ) and an offset frequency of  $200\text{ MHz}$ . Fig.5.11 shows the oscillation frequency of the LC-VCO with an without the added HFSN. The oscillation frequency, that is stable

Parameter	Symbol	Value
Tank Inductance	$L$	$1\text{ nH}$
Tank Capacitance	$C$	$1\text{ pF}$
Tank Resistance	$R$	$1\text{ k}\Omega$
Biasing Current	$I_D$	$5\text{ mA}$

Table 5.1. Base component values of the presented LC-VCO

when no noise is added, changes over time with the addition of noise in the tank, as predicted. The oscillation frequency follows a sinusoidal scheme with a modulation frequency of  $200\text{ MHz}$ , a maximum frequency deviation from the center frequency of  $361.3\text{ kHz}$ . Using the theory of frequency modulation [92], the amplitude of the sidebands in a frequency modulation can be calculated using 5.54, obtaining a sideband relative amplitude of  $-60.87\text{ dB}$ .

$$\text{Relative Sideband Amplitude FM} = -20 \cdot \log \left( 0.5 \cdot \frac{F_{dev}}{F_{mod}} \right) \quad (5.54)$$

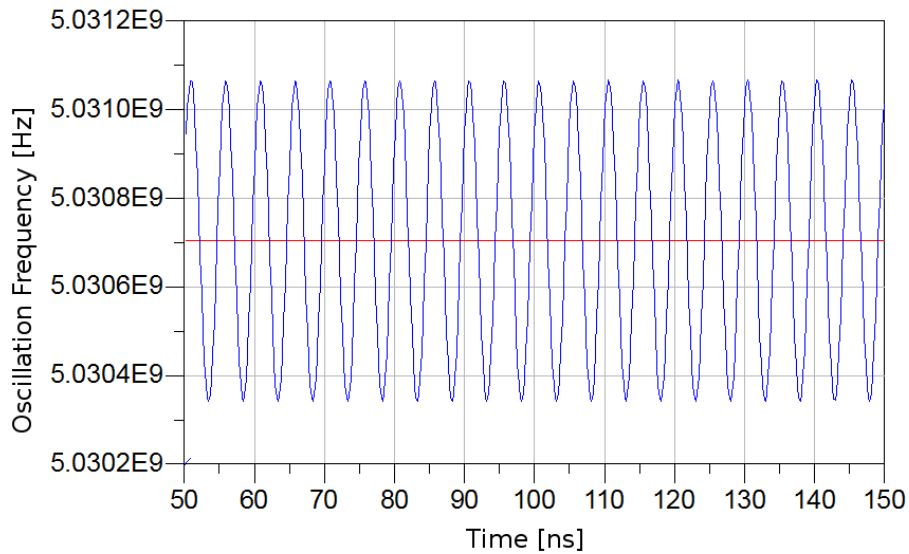


Figure 5.11. Oscillation Frequency with noise (blue trace) and without noise (red trace)

The results of this transient simulation can be compared with the results of the proposed model using (5.44), (5.45) and (5.53). The comparison between the obtained through simulation and

through the model are summarized in table.5.2, showing the excellent accuracy of the model in this particular case.

$$frequency\ Deviation = \frac{\omega_o}{2Q} \frac{A_i}{A_o} = \frac{5.03GHz}{2 \cdot 31.62} \frac{0.02}{4.46} = 356.9\ kHz \quad (5.55)$$

$$frequency\ Offset = (\omega_o - \omega_i) = 200\ MHz \quad (5.56)$$

$$\begin{aligned} RelativeSidebandAmplitude &= \quad (5.57) \\ &= 20 \cdot \log \left( 0.5 \cdot \left( \frac{A_i}{A_o} \frac{\omega_o}{2Q(\omega_o - \omega_i)} \right) \right) \\ &= 20 \cdot \log \left( 0.5 \cdot \left( \frac{0.02}{4.46} \frac{5.03GHz}{2 \cdot 31.62 \cdot 200MHz} \right) \right) \\ &= -60.99dB \end{aligned}$$

	Simulation	Model	Error
Modulation Frequency	200 MHz	200 MHz	NA
Frequency Deviation	361.3 kHz	356.9 kHz	1.23 %
Rel. Sideband Amplitude	-60.87 dB	-60.99 dB	0.12 dB

Table 5.2. Comparison between simulation and model prediction

This first example has shown that the oscillation frequency of the LC-VCO is frequency modulated by the injected noise and that the proposed model can accurately predict the behavior of the frequency modulated signal. In order to generalize the performed analysis, all the key parameters that, according to the proposed model, affect the performance of the LC-VCO will be analyzed individually. A simulation testbench has been designed to check their influence through simulations and to determine the numerical accuracy of the proposed model (5.53) to predict the effect of the frequency offset on the LC-VCO. The LC-VCO presented in Fig.5.8 is simulated using the base parameters shown in table 5.1. Some of these parameters were swept as variables in the simulations to analyze each of the key parameters.

### 5.4.2.1 Analysis of the effect of frequency offset

The analysis presented in this chapter has concluded that the frequency offset between the natural oscillation frequency of the LC-VCO and the frequency of the HFSN has a key influence on the degradation of the LC-VCO performance. The amplitude of the generated sidebands on the output spectrum of the LC-VCO suffers a decay of  $20 \text{ dB/dec}$  with respect to the frequency offset. The LC-VCO presented in Fig.5.8 is simulated for a wide range of the frequency of the noise sources. The frequency deviation and the amplitude of the sidebands are calculated from the simulation results. The results of the frequency offset simulation are summarized in table 5.3. Table 5.4 shows the results obtained from the model together with a comparison of these results with the results obtained with the simulations. Finally, the simulation and model results are shown graphically in Fig.5.12. The simulation results confirm the  $20 \text{ dB/dec}$  showing a very high accuracy both predicting the frequency deviation of the center frequency and the sideband amplitude. The relative error in the prediction of the frequency deviation is under 5 % which represents an error of less than  $0.5 \text{ dB}$  in the relative sideband amplitude prediction.

Freq offset	Osc Freq	Q	Osc Ampl	Noise Ampl	Freq Dev	Rel Sideband Ampl
20 MHz	5.03 GHz	31.6	4.46 $V_p$	10 mV <sub>p</sub>	357.7 kHz	-40.97 dB
50 MHz	5.03 GHz	31.6	4.41 $V_p$	10 mV <sub>p</sub>	358.2 kHz	-48.92 dB
100 MHz	5.03 GHz	31.6	4.44 $V_p$	10 mV <sub>p</sub>	360.7 kHz	-54.88 dB
200 MHz	5.03 GHz	31.6	4.46 $V_p$	10 mV <sub>p</sub>	361.3 kHz	-60.88 dB
500 MHz	5.03 GHz	31.6	4.43 $V_p$	10 mV <sub>p</sub>	369.8 kHz	-68.64 dB
1000 MHz	5.03 GHz	31.6	4.43 $V_p$	10 mV <sub>p</sub>	366.7 kHz	-74.73 dB
2000 MHz	5.03 GHz	31.6	4.43 $V_p$	10 mV <sub>p</sub>	341.3 kHz	-81.38 dB

Table 5.3. Simulation results of the effect of the frequency offset

Freq offset	Simulated Freq Dev	Model Freq Dev	Rel Error
20 $MHz$	357.7 $kHz$	356.6 $kHz$	0.3 %
50 $MHz$	358.2 $kHz$	361.2 $kHz$	0.8 %
100 $MHz$	360.7 $kHz$	358.3 $kHz$	0.7 %
200 $MHz$	361.3 $kHz$	357.3 $kHz$	1.1 %
500 $MHz$	369.8 $kHz$	359.3 $kHz$	2.8 %
1000 $MHz$	366.7 $kHz$	359.5 $kHz$	2.0 %
2000 $MHz$	341.3 $kHz$	359.5 $kHz$	5.3 %

---

Freq offset	Simulated Sb Ampl	Model Sb Ampl	Error
20 $MHz$	-40.97 $dB$	-41.00 $dB$	0.03 $dB$
50 $MHz$	-48.92 $dB$	-48.85 $dB$	0.07 $dB$
100 $MHz$	-54.88 $dB$	-54.94 $dB$	0.06 $dB$
200 $MHz$	-60.88 $dB$	-60.98 $dB$	0.10 $dB$
500 $MHz$	-68.64 $dB$	-68.89 $dB$	0.25 $dB$
1000 $MHz$	-74.73 $dB$	-74.91 $dB$	0.18 $dB$
2000 $MHz$	-81.38 $dB$	-80.93 $dB$	0.45 $dB$

Table 5.4. Comparison between simulation and model results of the effect of the frequency offset

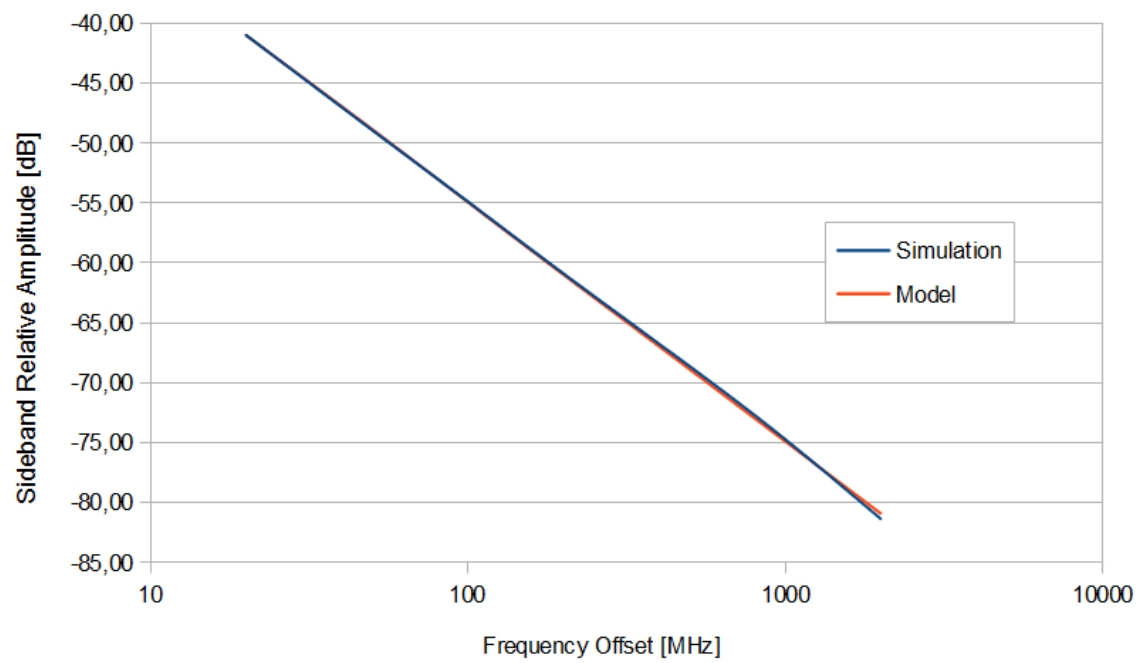


Figure 5.12. Comparison between the simulated and the model predicted relative sideband amplitude

#### 5.4.2.2 Analysis of the effect of the noise amplitude.

The frequency deviation and the relative sideband amplitude should present a direct proportionality with the noise amplitude. The simulation results, table 5.5 and Fig. 5.13, confirm this proportionality with a  $20 \text{ dB/dec}$  relationship between the relative sideband amplitude and the noise amplitude. The comparison between the results from simulation and model, table 5.6, shows a very high accuracy both predicting the frequency deviation of the center frequency and the sideband amplitude. The relative error in the prediction of the frequency deviation is under 2 % which represents an error of less than 0.2 dB in the relative sideband amplitude prediction.

Noise Ampl	Osc Freq	Freq Offset	Q	Osc Ampl	Freq Dev	Rel Sideband Ampl
0.001 $V_p$	5.03 GHz	200 MHz	31.6	4.33 $V_p$	36.4 kHz	-80.82 dB
0.002 $V_p$	5.03 GHz	200 MHz	31.6	4.34 $V_p$	72.8 kHz	-74.80 dB
0.005 $V_p$	5.03 GHz	200 MHz	31.6	4.34 $V_p$	182.0 kHz	-66.84 dB
0.01 $V_p$	5.03 GHz	200 MHz	31.6	4.43 $V_p$	364.1 kHz	-60.82 dB
0.02 $V_p$	5.03 GHz	200 MHz	31.6	4.43 $V_p$	728.2 kHz	-54.80 dB
0.05 $V_p$	5.03 GHz	200 MHz	31.6	4.43 $V_p$	1820.8 kHz	-46.84 dB
0.1 $V_p$	5.03 GHz	200 MHz	31.6	4.46 $V_p$	3643.0 kHz	-40.81 dB

Table 5.5. Simulation results of the effect of the tank noise amplitude



Noise Ampl	Simulated Freq Dev	Model Freq Dev	Rel Error
$0.001 V_p$	$36.4 \text{ kHz}$	$36.7 \text{ kHz}$	$0.9 \%$
$0.002 V_p$	$72.8 \text{ kHz}$	$73.3 \text{ kHz}$	$0.8 \%$
$0.005 V_p$	$182.0 \text{ kHz}$	$183.5 \text{ kHz}$	$0.8 \%$
$0.01 V_p$	$364.1 \text{ kHz}$	$359.7 \text{ kHz}$	$1.2 \%$
$0.02 V_p$	$728.2 \text{ kHz}$	$718.6 \text{ kHz}$	$1.3 \%$
$0.05 V_p$	$1820.8 \text{ kHz}$	$1797.3 \text{ kHz}$	$1.3 \%$
$0.1 V_p$	$3643.0 \text{ kHz}$	$3570.4 \text{ kHz}$	$2.0 \%$

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Noise Ampl	Simulated Sb Ampl	Model Sb Ampl	Error
$0.001 V_p$	$-80.82 \text{ dB}$	$-80.74 \text{ dB}$	$0.08 \text{ dB}$
$0.002 V_p$	$-74.80 \text{ dB}$	$-74.73 \text{ dB}$	$0.07 \text{ dB}$
$0.005 V_p$	$-66.84 \text{ dB}$	$-66.77 \text{ dB}$	$0.07 \text{ dB}$
$0.01 V_p$	$-60.82 \text{ dB}$	$-60.92 \text{ dB}$	$0.10 \text{ dB}$
$0.02 V_p$	$-54.80 \text{ dB}$	$-54.91 \text{ dB}$	$0.11 \text{ dB}$
$0.05 V_p$	$-46.84 \text{ dB}$	$-46.95 \text{ dB}$	$0.11 \text{ dB}$
$0.1 V_p$	$-40.81 \text{ dB}$	$-40.99 \text{ dB}$	$0.18 \text{ dB}$

Table 5.6. Comparison between simulation and model results of the effect of the tank noise amplitude

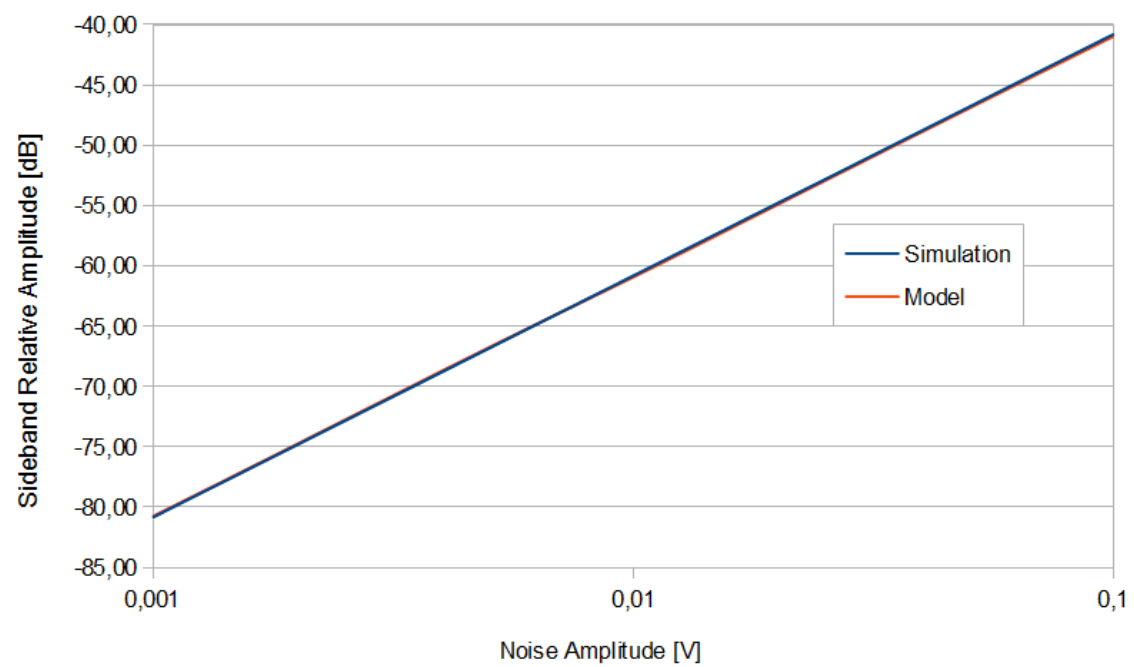


Figure 5.13. Comparison between the simulated and the model predicted relative sideband amplitude

### 5.4.2.3 Analysis of the effect of the oscillation amplitude.

The frequency deviation and the relative sideband amplitude should present an inverse proportionality with the oscillation amplitude. The oscillation amplitude can be changed with the VCO polarization current,  $I_{bias}$ , as shown in Fig. 5.14. The simulation results, table 5.7 and Fig. 5.15, confirm this inverse proportionality with a  $20 \text{ dB/dec}$  relationship between the relative sideband amplitude and the oscillation amplitude. The comparison between the results from simulation and model, table 5.8, shows a very high accuracy both predicting the frequency deviation of the center frequency and the sideband amplitude. The relative error in the prediction of the frequency deviation is under 3 % which represents an error of less than  $0.3 \text{ dB}$  in the relative sideband amplitude prediction. It is important to note that an ideal current source ( $I_{DC}$ ) has been used in this simulation. Consequently, the oscillation amplitude is not limited by the supply voltage and only depends on the oscillator tank and gain (this is the reason of the unusual high oscillation amplitudes presented here). Although this behavior differs from the one of a real oscillator, it is very handy for this investigation.

Osc Ampl	Noise Ampl	Osc Freq	Freq Offset	Q	Freq Dev	Rel Sideband Ampl
$4.44 V_p$	$0.01 V_p$	$5.03 \text{ GHz}$	$200 \text{ MHz}$	31.6	$361.8 \text{ kHz}$	$-60.87 \text{ dB}$
$7.59 V_p$	$0.01 V_p$	$5.03 \text{ GHz}$	$200 \text{ MHz}$	31.6	$212.6 \text{ kHz}$	$-65.49 \text{ dB}$
$10.70 V_p$	$0.01 V_p$	$5.03 \text{ GHz}$	$200 \text{ MHz}$	31.6	$150.9 \text{ kHz}$	$-68.47 \text{ dB}$
$13.82 V_p$	$0.01 V_p$	$5.03 \text{ GHz}$	$200 \text{ MHz}$	31.6	$117.6 \text{ kHz}$	$-70.63 \text{ dB}$
$16.93 V_p$	$0.01 V_p$	$5.03 \text{ GHz}$	$200 \text{ MHz}$	31.6	$96.0 \text{ kHz}$	$-72.40 \text{ dB}$
$20.05 V_p$	$0.01 V_p$	$5.03 \text{ GHz}$	$200 \text{ MHz}$	31.6	$81.5 \text{ kHz}$	$-73.82 \text{ dB}$
$23.17 V_p$	$0.01 V_p$	$5.03 \text{ GHz}$	$200 \text{ MHz}$	31.6	$70.7 \text{ kHz}$	$-75.05 \text{ dB}$

Table 5.7. Simulation results of the effect of the oscillation amplitude

Osc Ampl	Simulated Freq Dev	Model Freq Dev	Rel Error
4.437 $V_p$	36.4 $kHz$	361.8 $kHz$	0.8 %
7.590 $V_p$	72.8 $kHz$	212.6 $kHz$	1.3 %
10.704 $V_p$	182.0 $kHz$	150.9 $kHz$	1.4 %
13.816 $V_p$	364.1 $kHz$	117.6 $kHz$	2.0 %
16.931 $V_p$	728.2 $kHz$	96.0 $kHz$	2.0 %
20.049 $V_p$	1820.8 $kHz$	81.5 $kHz$	2.5 %
23.171 $V_p$	3643.0 $kHz$	70.7 $kHz$	2.8 %

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Osc Ampl	Simulated Sb Ampl	Model Sb Ampl	Error
4.437 $V_p$	-60.87 $dB$	-60.94 $dB$	0.07 $dB$
7.590 $V_p$	-65.49 $dB$	-65.60 $dB$	0.11 $dB$
10.704 $V_p$	-68.47 $dB$	-68.59 $dB$	0.12 $dB$
13.816 $V_p$	-70.63 $dB$	-70.81 $dB$	0.16 $dB$
16.931 $V_p$	-72.40 $dB$	-72.57 $dB$	0.17 $dB$
20.049 $V_p$	-73.82 $dB$	-74.04 $dB$	0.22 $dB$
23.171 $V_p$	-75.05 $dB$	-75.30 $dB$	0.25 $dB$

Table 5.8. Comparison between simulation and model results of the effect of the oscillation amplitude

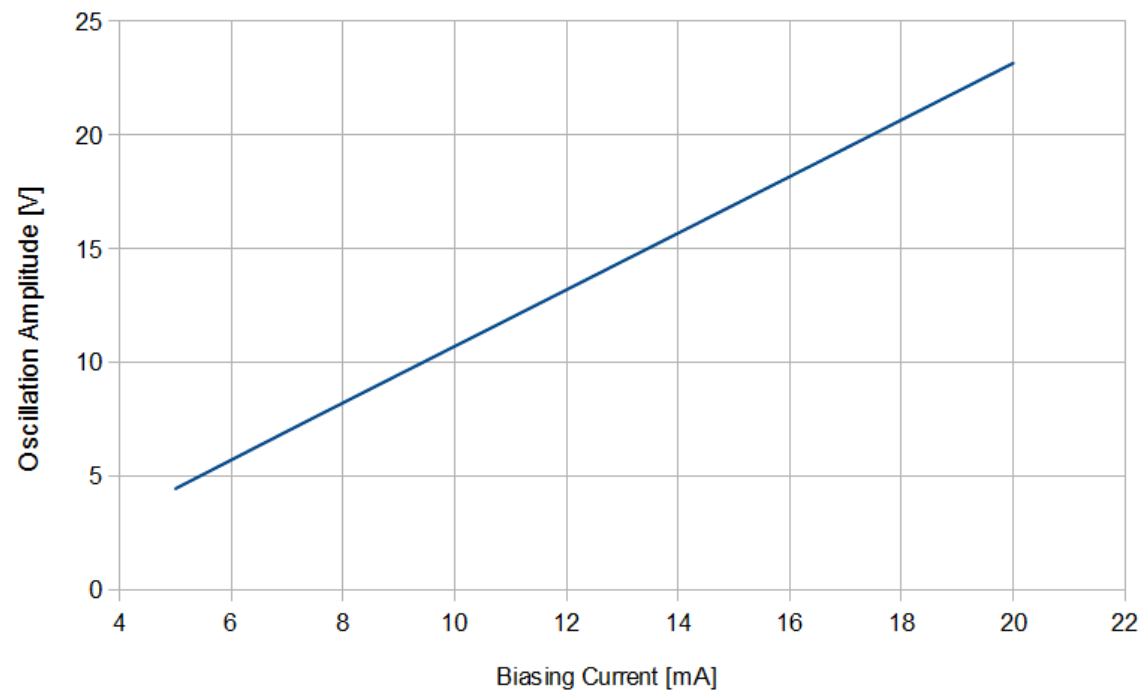


Figure 5.14. Relationship between biasing current and oscillation amplitude

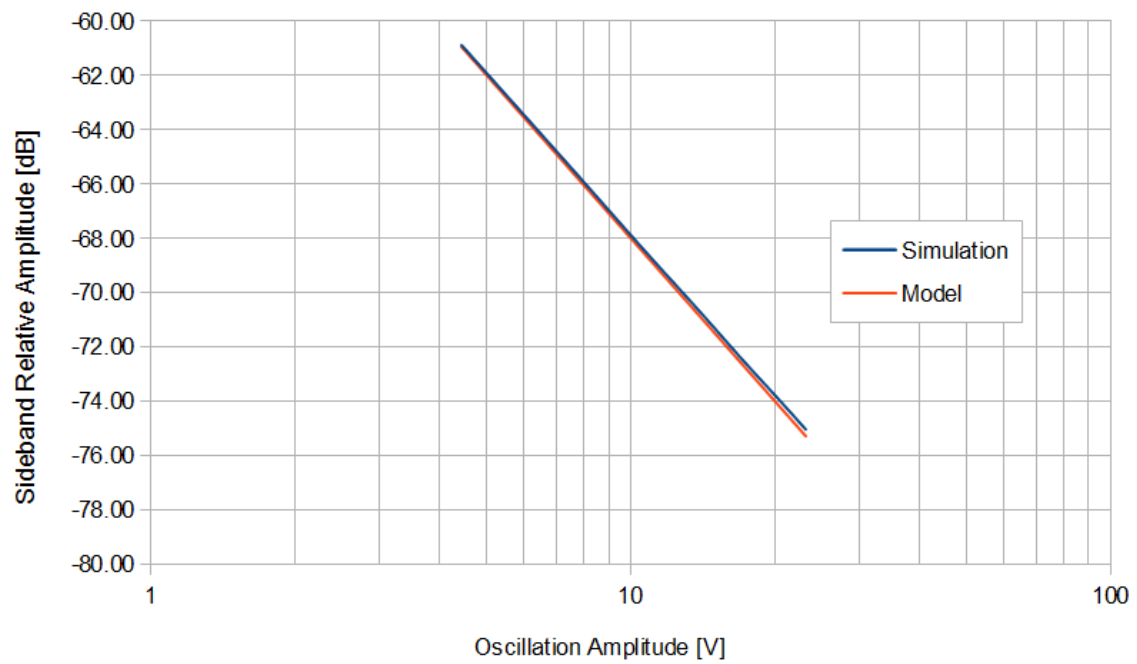


Figure 5.15. Comparison between the simulated and the model predicted relative sideband amplitude

#### 5.4.2.4 Analysis of the effect of the tank quality factor.

The frequency deviation and the relative sideband amplitude should present an inverse proportionality with the tank quality factor. The quality factor depends on the value of the tank parallel resistance,  $R_{par}$ . The main problem of changing the tank quality factor is that it also has a direct effect on the oscillator amplitude of the LC-VCO. In order to compensate that effect, the oscillator has been tuned, through  $I_{bias}$ , in order to keep the oscillation amplitude at the same value for all the analyzed tank quality factors. Fig.5.16 shows the relationship between the tank parallel resistance, the tank quality factor and the corresponding  $I_{bias}$ . The simulation results, table 5.10 and Fig. 5.17, confirm the inverse proportionality with a  $20\text{ dB/dec}$  relationship between the relative sideband amplitude and the tank quality factor. The comparison between the results from simulation and model, table 5.11, shows a very high accuracy both predicting the frequency deviation of the center frequency and the sideband amplitude. The relative error in the prediction of the frequency deviation is under 3 % which represents an error of less than  $0.3\text{ dB}$  in the relative sideband amplitude prediction.

Tank resistance	Tank Quality Factor	Bias current	Osc Amplitude
200 $\Omega$	6.32	73.30 $\text{mA}$	4.35 $V_p$
400 $\Omega$	12.65	21.05 $\text{mA}$	4.43 $V_p$
600 $\Omega$	18.97	8.73 $\text{mA}$	4.37 $V_p$
800 $\Omega$	25.30	6.86 $\text{mA}$	4.36 $V_p$
1000 $\Omega$	31.62	4.97 $\text{mA}$	4.41 $V_p$
1200 $\Omega$	37.95	3.83 $\text{mA}$	4.38 $V_p$
1400 $\Omega$	44.27	3.11 $\text{mA}$	4.38 $V_p$
1600 $\Omega$	50.60	2.61 $\text{mA}$	4.38 $V_p$

Table 5.9. Quality factor, bias current and oscillation amplitude for different values of the parallel tank resistance

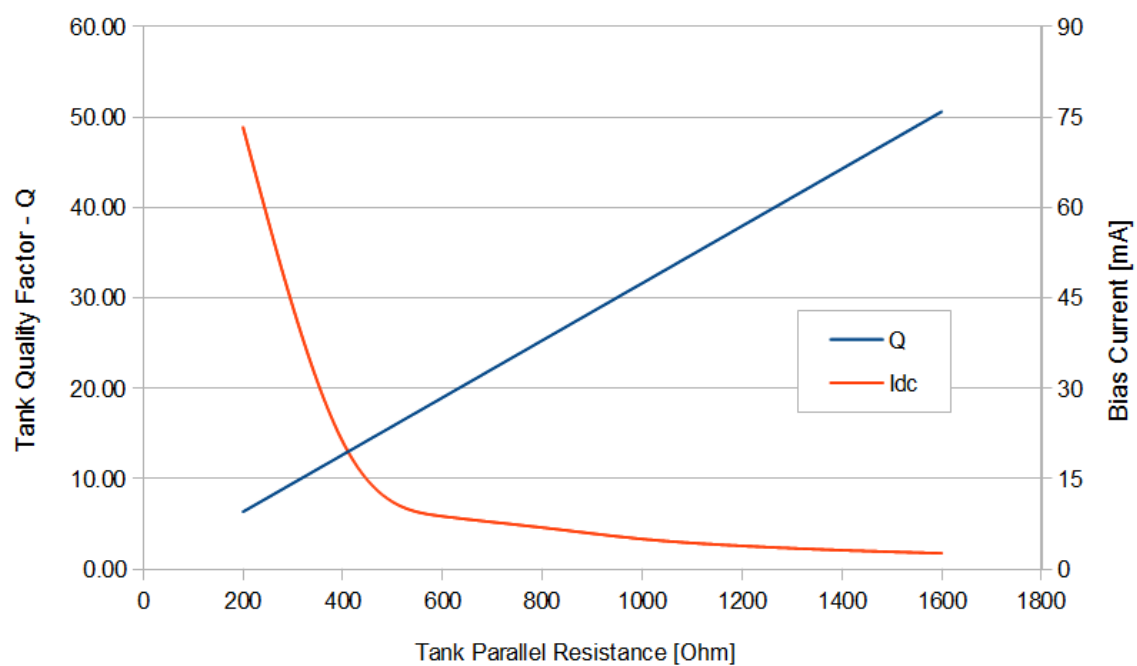


Figure 5.16. Relationship between the tank resistance, the biasing current and the tank quality factor

Q	Osc Freq	Freq Offset	Osc Ampl	Noise Ampl	Freq Dev	Sideband Ampl
6.32	5.032 GHz	200 MHz	4.35 V <sub>p</sub>	10 mV <sub>p</sub>	1874.2 kHz	-46.58 dB
12.65	5.032 GHz	200 MHz	4.43 V <sub>p</sub>	10 mV <sub>p</sub>	919.4 kHz	-52.77 dB
18.97	5.032 GHz	200 MHz	4.37 V <sub>p</sub>	10 mV <sub>p</sub>	620.3 kHz	-56.19 dB
25.30	5.032 GHz	200 MHz	4.36 V <sub>p</sub>	10 mV <sub>p</sub>	465.7 kHz	-58.68 dB
31.62	5.032 GHz	200 MHz	4.41 V <sub>p</sub>	10 mV <sub>p</sub>	370.2 kHz	-60.67 dB
37.95	5.032 GHz	200 MHz	4.38 V <sub>p</sub>	10 mV <sub>p</sub>	311.0 kHz	-62.19 dB
44.27	5.032 GHz	200 MHz	4.38 V <sub>p</sub>	10 mV <sub>p</sub>	266.7 kHz	-63.52 dB
50.60	5.032 GHz	200 MHz	4.38 V <sub>p</sub>	10 mV <sub>p</sub>	234.1 kHz	-64.65 dB

Table 5.10. Simulation results of the effect of the tank quality factor

Q	Simulated Freq Dev	Model Freq Dev	Rel Error
6.32	1874.2 <i>kHz</i>	1830.4 <i>kHz</i>	2.3 %
12.65	919.4 <i>kHz</i>	897.9 <i>kHz</i>	2.3 %
18.97	620.3 <i>kHz</i>	607.0 <i>kHz</i>	2.1 %
25.30	465.7 <i>kHz</i>	456.2 <i>kHz</i>	2.0 %
31.62	370.2 <i>kHz</i>	360.9 <i>kHz</i>	2.5 %
37.95	311.0 <i>kHz</i>	302.7 <i>kHz</i>	2.7 %
44.27	266.7 <i>kHz</i>	259.5 <i>kHz</i>	2.7 %
50.60	234.1 <i>kHz</i>	227.0 <i>kHz</i>	3.0 %
Q	Simulated Sb Ampl	Model Sb Ampl	Error
6.32	-46.58 <i>dB</i>	-46.79 <i>dB</i>	0.21 <i>dB</i>
12.65	-52.77 <i>dB</i>	-52.98 <i>dB</i>	0.22 <i>dB</i>
18.97	-56.19 <i>dB</i>	-56.38 <i>dB</i>	0.19 <i>dB</i>
25.30	-58.68 <i>dB</i>	-58.86 <i>dB</i>	0.18 <i>dB</i>
31.62	-60.67 <i>dB</i>	-60.89 <i>dB</i>	0.22 <i>dB</i>
37.95	-62.19 <i>dB</i>	-62.42 <i>dB</i>	0.23 <i>dB</i>
44.27	-63.52 <i>dB</i>	-63.76 <i>dB</i>	0.24 <i>dB</i>
50.60	-64.65 <i>dB</i>	-64.92 <i>dB</i>	0.27 <i>dB</i>

Table 5.11. Comparison between simulation and model results of the effect of the parallel tank resistance



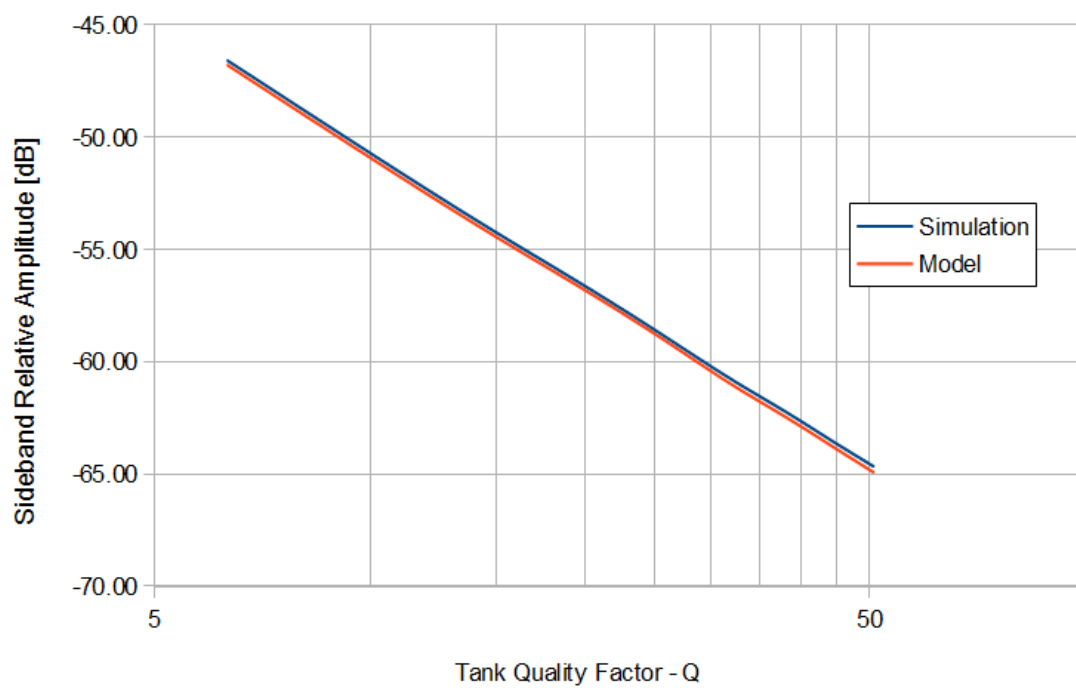


Figure 5.17. Comparison between the simulated and the model predicted relative sideband amplitude

#### 5.4.2.5 Analysis of the effect of the oscillation frequency.

Finally, the frequency deviation and the relative sideband amplitude should present a direct proportionality with the oscillation frequency. The oscillator frequency has been modified through the value of the tank inductance. The main problem of changing the oscillation frequency is that it also has a direct effect on the quality factor and, so, on the oscillation amplitude of the LC-VCO. It is easy to maintain constant the value of the tank quality factor as it is inversely proportional of the value of the inductance. The oscillation amplitude has been tuned using the same method than in the quality factor case. Table 5.12 shows the relationship between the oscillation frequency, the required tank parallel resistance and bias current to hold  $Q$  and the oscillation amplitude constants. The simulation results, table 5.13 and Fig. 5.18, confirm the direct proportionality with a  $20\text{ dB/dec}$  relationship between the relative sideband amplitude and the oscillation frequency. The comparison between the results from simulation and model, table 5.14, shows a very high accuracy both predicting the frequency deviation of the center frequency and the sideband amplitude. The relative error in the prediction of the frequency deviation is under 2 % which represents an error of less than 0.15 dB in the relative sideband amplitude prediction.

Oscillation frequency	Tank resistance	Bias current	Osc Amplitude	Q
1.0 GHz	4876.0 $\Omega$	0.73 mA	4.38 $V_p$	31.6
2.0 GHz	2476.4 $\Omega$	1.52 mA	4.37 $V_p$	31.6
3.0 GHz	1659.6 $\Omega$	2.52 mA	4.45 $V_p$	31.6
4.0 GHz	1248.0 $\Omega$	3.64 mA	4.39 $V_p$	31.6
5.0 GHz	1000.0 $\Omega$	4.93 mA	4.35 $V_p$	31.6
6.0 GHz	834.2 $\Omega$	6.44 mA	4.35 $V_p$	31.6

Table 5.12. Parallel tank resistance, bias current and oscillation amplitude for different values of the oscillation frequency

Osc Freq	Q	Osc Ampl	Noise Ampl	Freq Dev	Sideband Ampl
1.0 GHz	31.6	4.38 V <sub>p</sub>	10 mV <sub>p</sub>	75.8 kHz	-74.45 dB
2.0 GHz	31.6	4.37 V <sub>p</sub>	10 mV <sub>p</sub>	149.2 kHz	-68.57 dB
3.0 GHz	31.6	4.45 V <sub>p</sub>	10 mV <sub>p</sub>	219.2 kHz	-65.22 dB
4.0 GHz	31.6	4.39 V <sub>p</sub>	10 mV <sub>p</sub>	294.5 kHz	-62.66 dB
5.0 GHz	31.6	4.35 V <sub>p</sub>	10 mV <sub>p</sub>	371.3 kHz	-60.65 dB
6.0 GHz	31.6	4.35 V <sub>p</sub>	10 mV <sub>p</sub>	442.6 kHz	-59.12 dB

Table 5.13. Simulation results of the effect of the oscillation frequency

Osc Freq	Simulated Freq Dev	Model Freq Dev	Rel Error
1.0 GHz	75.8 kHz	74.5 kHz	1.7 %
2.0 GHz	149.2 kHz	147.1 kHz	1.4 %
3.0 GHz	219.2 kHz	215.5 kHz	1.7 %
4.0 GHz	294.5 kHz	290.5 kHz	1.4 %
5.0 GHz	371.3 kHz	365.8 kHz	1.5 %
6.0 GHz	442.6 kHz	438.5 kHz	0.9 %

Osc Freq	Simulated Sb Ampl	Model Sb Ampl	Error
1.0 GHz	-74.45 dB	-74.60 dB	0.15 dB
2.0 GHz	-68.57 dB	-68.69 dB	0.14 dB
3.0 GHz	-65.22 dB	-65.37 dB	0.15 dB
4.0 GHz	-62.66 dB	-62.78 dB	0.12 dB
5.0 GHz	-60.65 dB	-60.78 dB	0.13 dB
6.0 GHz	-59.12 dB	-59.20 dB	0.08 dB

Table 5.14. Comparison between simulation and model results of the effect of the oscillation frequency

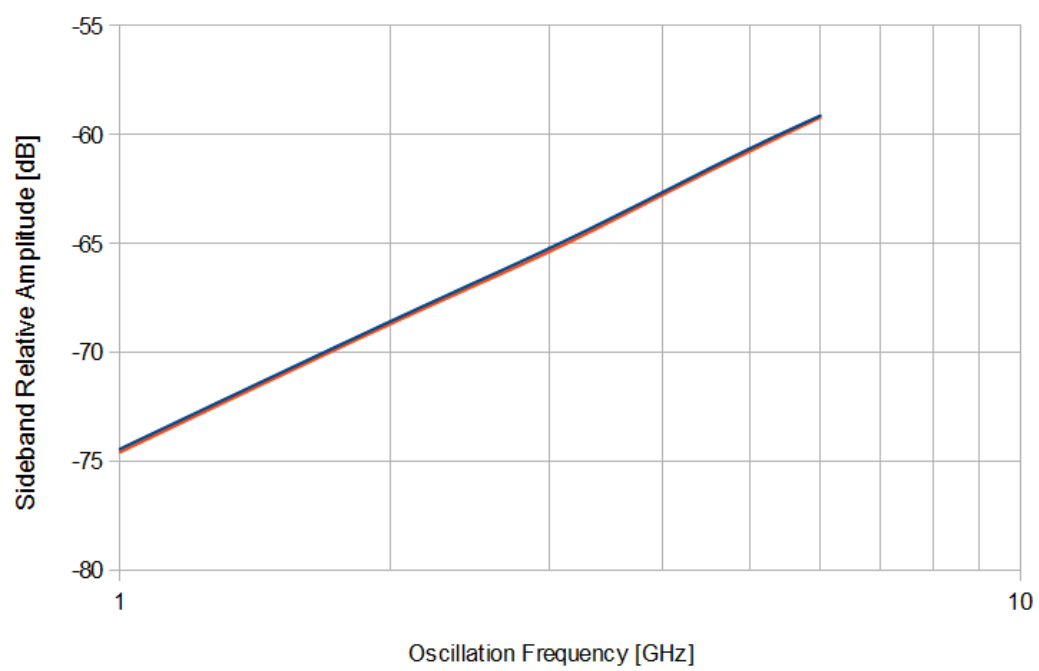


Figure 5.18. Comparison between the simulated and the model predicted relative sideband amplitude

## 5.5 Summary and conclusions

Chapter 4 showed the effect of HFSN on an LC-VCO from real measurements. A cause of the LC-VCO output degradation was hypothesized based on the empirical analysis: frequency pulling. This chapter has faced the analysis of the effect of HFSN on an LC-VCO from a theoretical point of view. The theoretical analysis has also been supported by simulations.

The presented analysis has exploited the distinctive features of the scenario where the HFSN reaching the oscillator has an small amplitude compared to the amplitude of the oscillator and a frequency very close to the oscillation frequency, to reduce the high complexity of the theory around unlocked injection locked oscillators. This analysis has led to a practical model of the degradation of the LC-VCO performance due to HFSN based on the parameters and characteristics of the LC-VCO (oscillation amplitude, oscillation frequency and tank quality factor) and of the HFSN (amplitude of the noise reaching the tank and frequency offset between the noise and the oscillator).

The conclusions obtained from the model show that the robustness of the oscillator improves through an increase of the tank quality factor, the oscillation amplitude or if the oscillation frequency decreases. By contrast, the HFSN becomes more harmful if the amount of noise reaching the tank increases or if the frequency offset between the oscillator and the noise decreases. These conclusions provided by the model match with the dependencies observed in the experimental measurements performed in chapter 4.

The model can correctly predict the observed dependencies, proving to be valid from a qualitative point of view but the evaluation of its quantitative accuracy faces a serious limitation: one of the main parameters of the model, the amount of noise that reaches the tank, is not available from the measurements. In order to circumvent this limitation, the quantitative accuracy of the model has been evaluated using the simulation results of an LC-VCO, which has been compared with the predictions of the model, showing an outstanding minimal error between model and simulation results.

As a conclusion, the proposed model has proven to be a very useful tool to evaluate the behavior of an LC-VCO in hostile HFSN environments. Moreover, the model can help system designers to predict the effect of HFSN and increase the robustness of their oscillators, showing them the design parameters that can be tuned or adjusted.



## Chapter 6

# Design of a 2.5 GHz QVCO robust against HFSN.

### 6.1 Introduction and objectives

A common receiver architecture to downconvert the information to lower frequencies is the use of very low intermediate frequencies or even zero-IF (direct conversion) [115], [117]. These architectures provide several advantages in terms of power consumption and ease to deal with the demodulated signal at low frequency. A common characteristic in these architectures is that all the subsystems (specially the oscillator and the PA) work at very similar frequencies causing a serious risk of oscillator pulling. At zero-IF or low-IF it is necessary to use a Quadrature Voltage Controlled Oscillator (QVCO) to generate the phase and quadrature components of the signal (I and Q). There are several options available to generate I and Q from an LC-VCO (cross coupled, polyphase), but one of them is the use of a frequency prescaler to divide the frequency of an LC-VCO running at twice the desired output frequency. This technique separates the frequency of the oscillator from the main system frequency, reducing the effect of pulling in the LC-VCO. This way, the interaction between the blocks is highly mitigated, as concluded from the analysis developed in previous chapters.

This chapter shows the design process of a QVCO following this strategy. A 2.5 GHz QVCO has been designed and manufactured using a 5 GHz LC-VCO and a frequency divider. Several techniques have been used, based on the proposed model, in order to maximize the robustness of the

oscillator to HFSN with a minimal effect on its characteristics. All the consequences and tradeoffs of using the modifications proposed by the model are deeply analyzed.

This chapter presents a detailed case study about how the proposed model can be extremely useful to optimize the performance of an oscillator in the presence of HFSN.

## 6.2 2.5 GHz design and measured performance

A 2.5 GHz QVCO has been designed using a frequency division technique in order to reduce the effect of HFSN on its performance. Fig. 6.1 shows the block diagram of the structure of the QVCO. The LC-VCO oscillates at the double of the desired frequency. The frequency divider divides this frequency by a factor of two and generates the phase and quadrature components. A diagram of the input and output differential signals of the frequency divider is shown in Fig. 6.2. Both, the practical observation shown in Fig.4.8 and the model developed back in chapter 5 suggest that this architecture should be practically immune to noise at 2.5 GHz due to the high frequency offset between this frequency and the LC-VCO oscillation frequency.

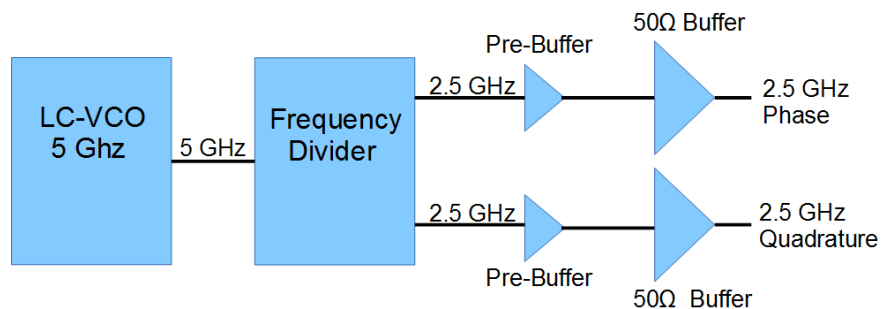


Figure 6.1. Structure of the 2.5 GHz QVCO

This section details the design process of both the LC-VCO and the frequency divider showing their measured characteristics. The integration between the two blocks is presented together with the measured performance of the complete 2.5 GHz QVCO.

### 6.2.1 5 GHz LC-VCO design

A Complementary MOS VCO topology has been chosen in order to reduce the power consumption and the phase noise of the LC-VCO. This structure, shown in Fig.6.3, uses two NMOS and two



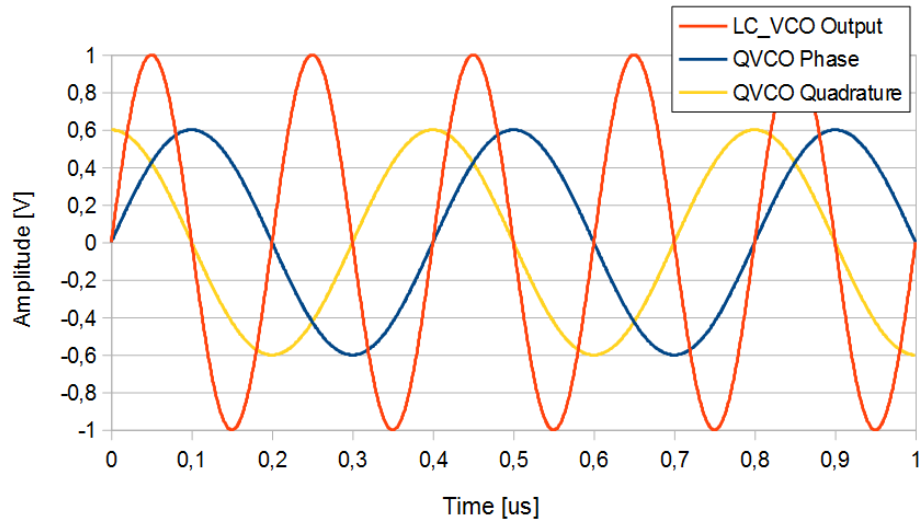


Figure 6.2. Diagram of the frequency divider input and output signals.

PMOS transistors to provide the required gain. It provides a larger output voltage swing and approximately 3 dBs of improved phase noise in comparison with the NMOS or PMOS topologies [86].

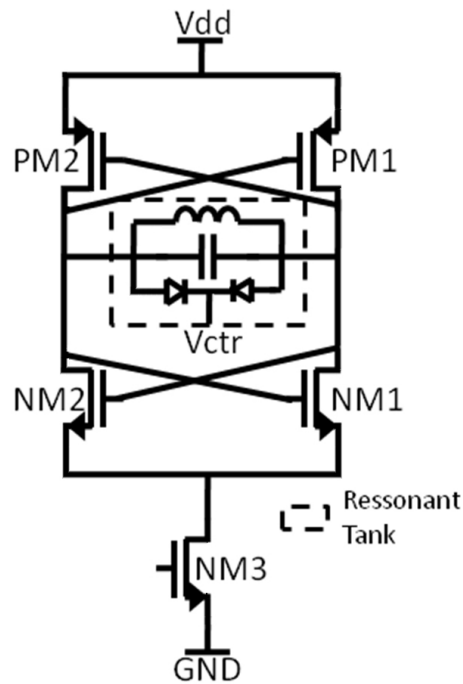


Figure 6.3. Schematic of the 5 GHz LC-VCO

The tank quality factor plays an important role in the performance of the LC-VCO. On the one hand, according to the Leeson model [118], [119], shown in (6.1), the magnitude of the VCO phase noise is directly related to the quality factor  $Q$  of the tank. On the other hand, the oscillation amplitude

of an LC-VCO has also a strong correlation with  $Q$ . For a fixed bias current, the output amplitude grows with  $Q$ ; for a fixed output amplitude, less current is required for higher  $Q$ s. Consequently, the tail transistor that provides this current can be made smaller and thus its contribution to noise reduced [86].

$$\mathcal{L}\{\Delta\omega\} = 10 \cdot \log_{10} \left\{ \frac{2FkT}{P_s} \left[ 1 + \left( \frac{\omega_o}{2Q\Delta\omega} \right)^2 \right] \right\} \quad (6.1)$$

The consequence of all these arguments is that the quality factor is a critical element on the design process of the 5 GHz LC-VCO. As shown in chapter 5, the tank quality factor is obtained from the combination of the quality factors of the capacitor and the inductor. At the ISM frequency bands the  $Q_L$  factor of the inductor is much lower than the capacitors and varactors  $Q_C$ , being then the tank  $Q$  factor mainly limited by that of the inductor. In order to maximize  $Q_L$ , in this design we have used a single layer square symmetric inductor of 1.5 turns made in the top metal layer of  $4.5 \mu m$  thickness<sup>1</sup>. The inductor is designed with a non-constant width to optimize the  $Q_L$  value at high frequencies [120]. Additionally, the high resistivity substrate ( $10 \Omega \cdot cm$ ) of the CMOS process allows a reduction of the high frequency substrate losses, contributing to increase the value of  $Q_L$  [65], [121].

One stand-alone inductor was manufactured in order to experimentally measure its characteristics and compare them with the performance predicted by the simulations done with Momentum. The measurements were done using an on-wafer passive GSGSG differential probe. Pad and interconnect parasitics were deembedded using a three step SOT method [122], [123]. The measurement results are shown in Fig.6.4, together with an image of the inductor layout. According to these measurements a  $Q_L$  factor above 9 is reached at the 5 GHz working frequency, while the inductance is  $L = 1.5 nH$ .

The LC-VCO tank is designed to resonate at a central frequency of 4.9 GHz and to have a minimum tuning range of 200 MHz (in order to fit the communication standards residing at the 2.4GHz ISM Band, like Bluetooth, WIFI or ZigBee). This tuning range is achieved with a varactor together with a bank of digitally switched capacitors, which provide a coarse adjustment to compensate for process variations. Each of these switched capacitors has been implemented using a MIM capacitor and an NMOS transistor acting as a switch. There are three binary scaled capacitors controlled by a word of three bits, allowing an output frequency change step of 60 MHz.

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<sup>1</sup>The inductor has been designed by the research group of Javier Sieiro and José María López-Villegas from the Electronics Dept. of the Universitat de Barcelona, Spain

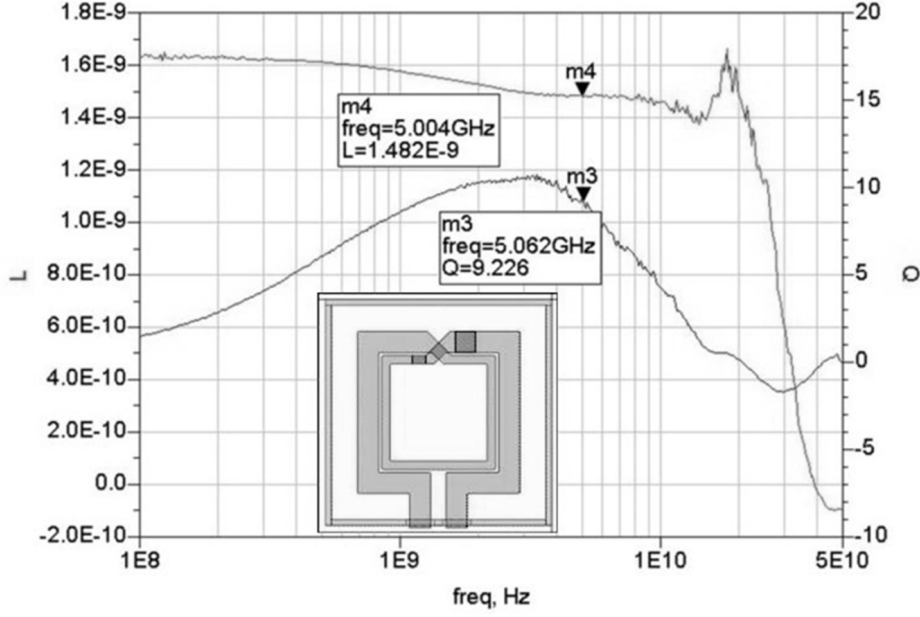


Figure 6.4.  $L$  and  $Q_L$  measurements, together with the inductor layout.

The parasitic capacitances of the transistors and interconnect lines must be considered during the design of an LC-VCO resonant tank, what is especially important in a complementary topology. In our case, parasitic capacitances produce a frequency deviation of  $80\text{ MHz}$  when included in the simulations. The parasitics were extracted after the design of the circuit layout, and then the fixed capacitance was re-sized in order to resonate with the tank inductance at the desired central frequency.

Regarding the design of the active devices, the cross-coupled transistors have been designed for a low value of  $V_{GS} - V_T$ , thus increasing their transconductance-to-current ratio and reducing the power consumption. Special care has been taken in the transistor sizing to ensure similar  $g_m$  for the NMOS and the PMOS transistors, increasing then the symmetry on the output waveform, which leads to a decrease in the phase noise [86]. The tail transistor has been designed keeping its W/L ratio as low as possible, which reduces the up-converted flicker noise [86].

### 6.2.2 Experimental characterization of the 5 GHz LC-VCO

Measurement results of the  $5\text{ GHz}$  oscillator alone show that the minimum required biasing current to start the oscillation is around  $400\text{ }\mu\text{A}$ . In order to have some design margin a biasing current of  $500\text{ }\mu\text{A}$  is used, what provides a  $250\text{ mV}_{pp}$  output signal for the VCO. The measured oscillation frequency for a full sweep of the control voltage shows to cover the full frequency range between  $4.8\text{ GHz}$  and  $5\text{ GHz}$  with a maximum sensitivity of  $1\text{ GHz/V}$ . The measured phase noise for

the extremely low power consumption of  $0.6\text{ mW}$  at  $1.2\text{ V}$  is only  $-109\text{ dBc/Hz}$  @  $1\text{ MHz}$  offset, thanks to the high quality factor of the tank and the chosen architecture. The performance of the LC-VCO is summarized in Table 6.1.

Parameter	Value
Technology	CMOS $0.18\text{ }\mu\text{m}$
Supply voltage	$1.2\text{ V}$
Power consumption	$0.6\text{ mW}$
Frequency tuning range	$4.7\text{ GHz} \rightarrow 5.1\text{ GHz}$
Maximum freq. tuning sensitivity	$1000\text{ MHz/V}$
Digital tuning range	$\pm 200\text{ MHz}$
Phase noise @ $1\text{ MHz}$	$-108.8\text{ dBc/Hz}$

Table 6.1. Summary of the measured  $5\text{ GHz}$  LC-VCO characteristics and performance

### 6.2.3 Frequency divider design

A frequency divider connected to the  $5\text{ GHz}$  LC-VCO output is responsible for the generation of the Quadrature (Q) and Phase (I) components of the  $2.5\text{ GHz}$  QVCO signals. The goal of this design process is to achieve the correct operation and the best I/Q balance with the minimum power consumption. The structure of the frequency divider is shown in Fig.6.5. It consists of two identical CML (Current Mode Logic) D-latches [124] connected in a master-slave scheme with negative feedback. The  $5\text{ GHz}$  signal, coming from the LC-VCO is connected to the clock input [125], [126]. The digital latches have been designed using CML logic in order to ensure enough switching speed using reasonable power. Fig.6.6 shows the transistor level schematic of one of the latches. The transistors and resistors of the latches must be properly sized to get the right operation at the desired frequency and with the minimum power consumption [127]. Moreover, the design of the divider is not independent of the  $5\text{ GHz}$  VCO, but presents some interesting trade-offs. This section details the sizing procedure of the divider in order to achieve a minimization of the overall  $2.5\text{ GHz}$  QVCO power consumption.

Dividers like that shown in Fig.6.5 can operate in two main regions: locked to the CLK input signal or in free running mode. Obviously, the frequency division is only obtained when the divider is locked to the CLK input signal. There is a minimum clock input amplitude for every input frequency

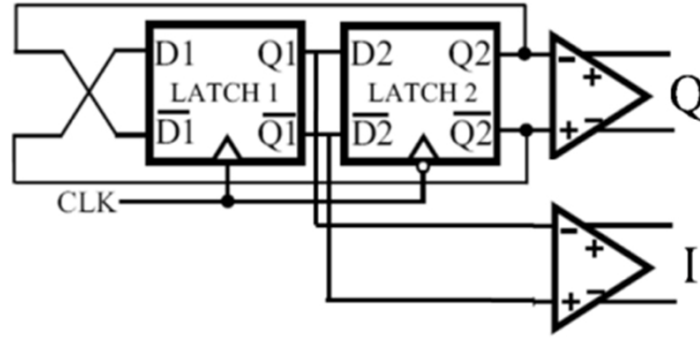


Figure 6.5. Structure of the frequency divider.

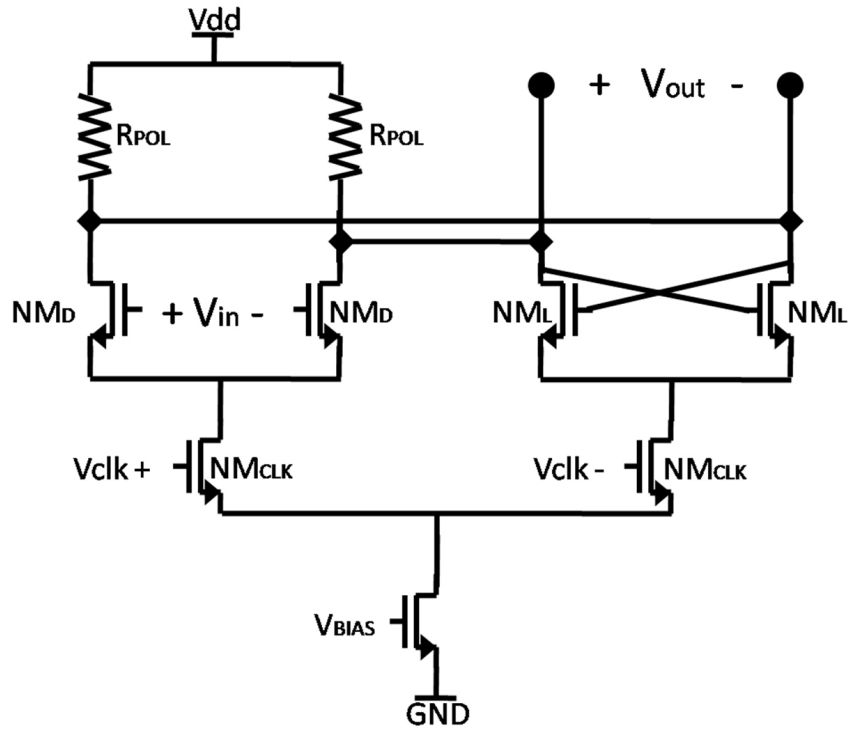


Figure 6.6. Schematic of one of the frequency divider latches.

that must be attained in order to lock the divider. This requirement is graphically represented by the sensitivity curve, showing the relationship between the CLK signal frequency, its amplitude and the oscillation mode of the divider. A typical sensitivity curve is shown in Fig.6.7.

In order to minimize the power consumption, since the  $5\text{ GHz}$  LC-VCO output amplitude depends on its current consumption, the locked oscillation region should be reached with the lowest possible CLK amplitude. According to the curve in Fig.6.7, the minimum required CLK amplitude is produced when the CLK frequency is twice the oscillation frequency of the divider when it operates in the free running mode (FSO). Both FSO and the slopes of the sensitivity curve around this

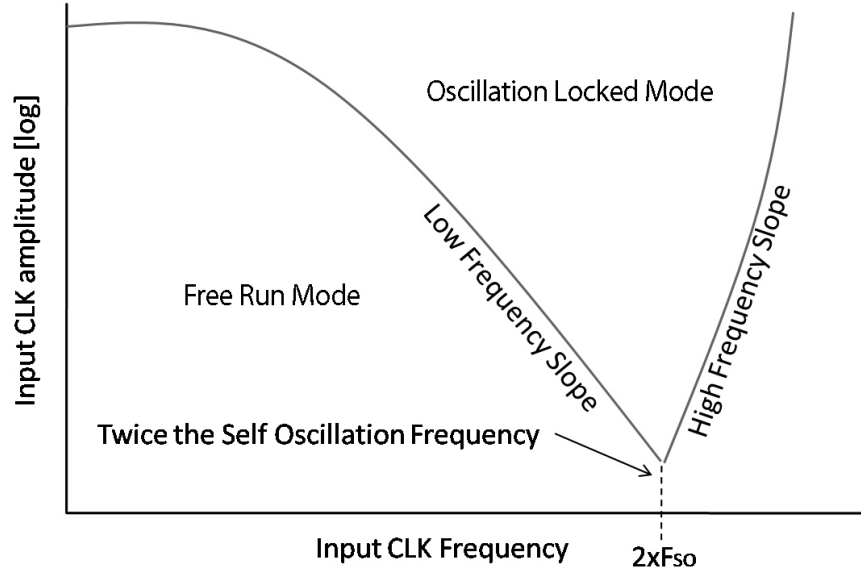


Figure 6.7. Typical sensitivity curve of a CML frequency divider.

point can be modified and optimized through the correct sizing of all the transistors and passive elements, the power consumption and the layout parasitics of the CML gates. The main objective of the optimization process is to obtain a  $2 \cdot F_{SO}$  value around the input clock frequency of  $5\text{ GHz}$  and to reduce the lateral slopes to relax the input amplitude requirements around this point while keeping the power consumption as low as possible. The cross coupled transistors (NML in Fig.6.6) are responsible for the switching process of the divider. They should have enough transconductance to compensate for the losses of the RPOL resistance, allowing the divider to oscillate. The oscillation condition is shown in (6.2).

$$g_{mNML} \cdot R_{POL} > 1 \quad (6.2)$$

If the size of the cross coupled transistors is increased the self oscillation and the maximum oscillation frequencies of the divider drops. Then, the size of these transistors should be minimized without breaking the oscillation condition. Once the size of NML is fixed, the driver transistors (NMD) are chosen to have a similar size because, as stated in [127], this allows to optimize (to reduce) the slope of the sensitivity curve around FSO. The size of the clock transistors (NMCLK) has been optimized to maximize the amount of energy transmitted from the clock input to the driver and to the cross-coupled transistors, thus reducing the required clock input voltage swing. This optimization depends on the biasing point of the clock input, which corresponds to the output biasing point of the  $5\text{ GHz}$  VCO (DC blocking capacitors are not used to reduce losses and parasitics in the signal

path). Increasing the size of these transistors improves the energy coupling between the clock input and the signal path but it also increases the parasitic capacitance, dramatically increasing the high frequency slope of the sensitivity curve, and thus limiting the high frequency operation of the divider. The biasing resistors (RPOL) have a high impact on the output waveform. Increasing the value of these resistors increases the output signal amplitude but it causes a drop in the DC bias voltage of the transistor chain, reducing the sensitivity to the clock signal. Such DC bias voltage drop can be compensated by increasing the power consumption of the divider, but this is obviously an undesired solution. The optimization of all these device parameters depends on the power consumption, since the overall behavior of the frequency divider can be improved by increasing the biasing current. As the power consumption increases, the  $2 \cdot F_{SO}$  point is pulled to higher frequencies, the slopes of the sensitivity curves are reduced, the output signal amplitude grows, and the impact of the layout parasitic is reduced. The measured sensitivity curve for the latches designed following the optimization criteria described above is shown in Fig.6.8. Note that the  $2 \cdot F_{SO}$  point has been set at  $4.5 \text{ GHz}$ , what is around  $0.5 \text{ GHz}$  below the frequency for the required band. The reduction of self-oscillation frequency reduces the power consumption of the divider but increases the amplitude requirement for the CLK signal, and consequently the power consumption of the  $5 \text{ GHz}$  VCO. The optimization of this trade-off leads to the minimum power consumption for the complete  $2.5 \text{ GHz}$  QVCO. With the chosen  $2 \cdot F_{SO}$  value, the divider presents a power consumption of  $1.4 \text{ mW}$  for a supply voltage of  $1.2 \text{ V}$ .

The divider design was completed by adding  $50 \Omega$  output buffers as shown in Fig.6.5. The output nodes of the latches are extremely sensitive to the load capacitance connected to them; therefore it is necessary to include intermediate pre-buffers (Fig.6.1) in order to have this loading effect under control. The pre-buffers have been designed using very small transistors in order to reduce their input capacitance.

#### 6.2.4 Experimental characterization of the 2.5 GHz QVCO

The  $2.5 \text{ GHz}$  QVCO has been built by connecting the  $5 \text{ GHz}$  LC-VCO output to the frequency divider clock input. This connection can be done without decoupling capacitors and without adding an input bias circuit because the frequency divider input bias voltage has been optimized to match the output bias voltage of the  $5 \text{ GHz}$  VCO. An image of the manufactured QVCO is shown in Fig.6.9,

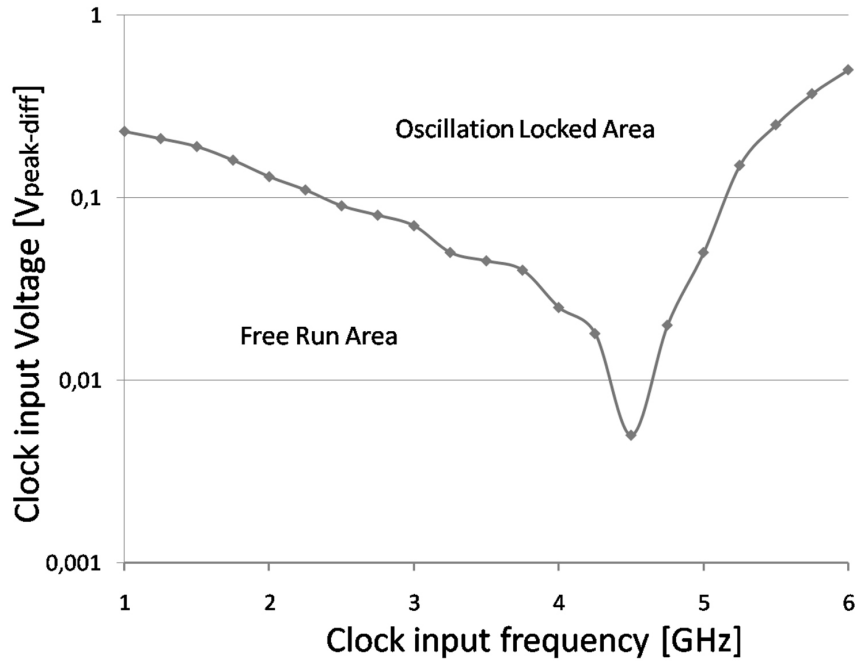


Figure 6.8. Measured sensitivity curve of the divider designed in this work.

where the GSGSG probes connected to the I and Q ports and the probes for biasing and DC control are also shown.

During the physical design phase, special care has been taken to equalize the parasitic capacitance of the interconnect lines, which play an important role in the final performance of the circuit, particularly regarding the I/Q balance. The four lines (I, Q) should have the same length and the same physical contour conditions. All the divider transistors have been strategically placed into the layout to maintain homogeneous lengths in the four signal paths. Dummy structures have been added to equalize the load of all the lines. They have been routed using the higher metal levels to reduce the parasitic capacitance and the coupling to the substrate.

Experimental measurements indicate an excellent performance of the QVCO. Measured power consumption was only  $2\text{ mW}$  from a  $1.2\text{ V}$  voltage supply. Note that this number does not include the consumption of the output buffers. Phase noise at the output of the  $2.5\text{ GHz}$  QVCO has been reduced by  $6\text{ dB}$  with respect to the value of the  $5\text{ GHz}$  LC-VCO due to the frequency division factor. The performance of the QVCO is summarized in Table 6.2. The characteristics of the  $2.5\text{ GHz}$  QVCO make it suitable for most of the low power communication standards in the  $2.5\text{ GHz}$  ISM band, like Bluetooth, Bluetooth LE or Zigbee.



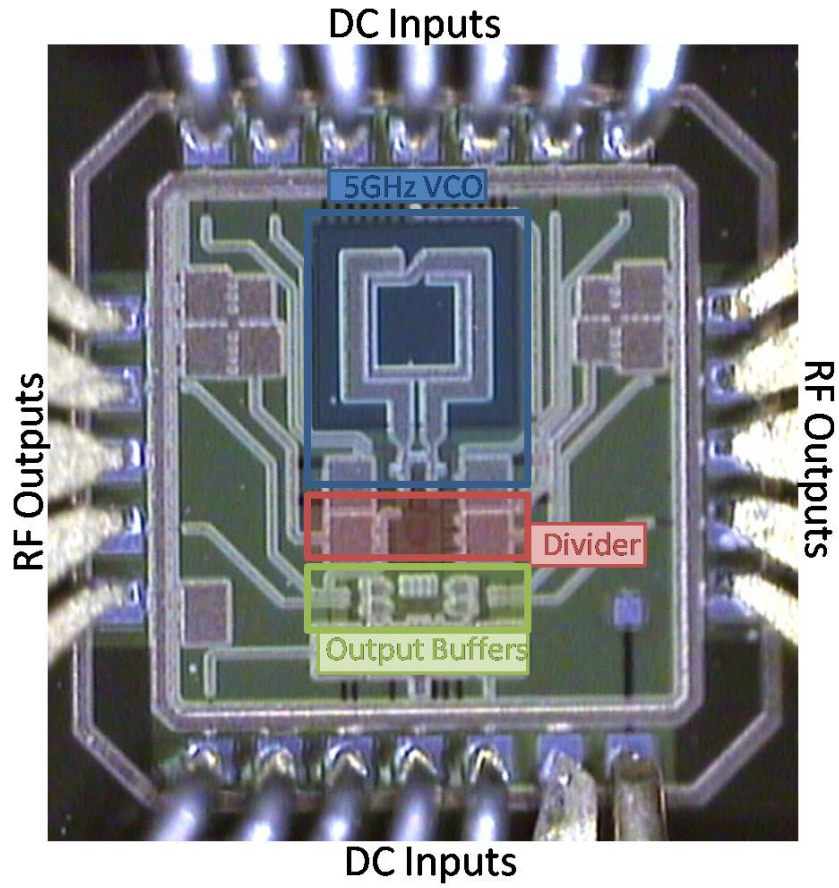


Figure 6.9. Micro photography of the manufactured QVCO

Parameter	Value
Technology	CMOS 0.18 $\mu m$
Supply voltage	1.2 V
Power consumption	2.0 mW
Frequency tuning range	2.35 GHz $\rightarrow$ 2.55 GHz
Maximum freq. tuning sensitivity	500 MHz/V
Digital tuning range	$\pm 100$ MHz
Phase noise @ 1 MHz	-114.8 dBc/Hz
I/Q phase unbalance	$< 2.5^\circ \pm 0.5^\circ$

Table 6.2. Summary of the measured 2.5 GHz QVCO characteristics and performance

### 6.3 Evaluation of the effect of HFSN on the 2.5 GHz QVCO

It has already been shown that the presented model is a useful tool that can identify the design variables that can be optimized in order to maximize the robustness of an LC-VCO to HFSN. This section presents and discusses the strategies followed and the measures taken to reduce the degradation of this particular QVCO.

One of the conclusions obtained from the presented model shows that the closer the substrate noise frequency to the LC-VCO output frequency, the higher the degradation of the output signal. In direct conversion systems, most of the RF blocks, like the Low Noise Amplifier (LNA), the Power Amplifier (PA), buffers, etc, work at the same frequency range as the oscillator, injecting lots of noise around its output frequency. The main purpose of the LC-VCO + frequency divider topology used in this design is to shift the LC-VCO frequency, and thus the noise sensitive frequencies, away from the frequency range with the strongest noise components. Nevertheless, robustness against the 2.5 GHz noise does not guarantee complete immunity of the QVCO against substrate noise, since noise components around 5 GHz can still affect the 5 GHz LC-VCO, and consequently degrade the 2.5 GHz QVCO output. This 5 GHz noise can be generated by high-order harmonics of the digital circuitry [10], or other parts of the RF circuitry, specially the PA, which, in a direct conversion architecture, will produce its second harmonic at the LC-VCO frequency [128]. As an example, Fig.6.10 shows the degradation of the output spectrum of the 5 GHz LC-VCO when a 10 dBm substrate noise tone is injected around its output frequency.

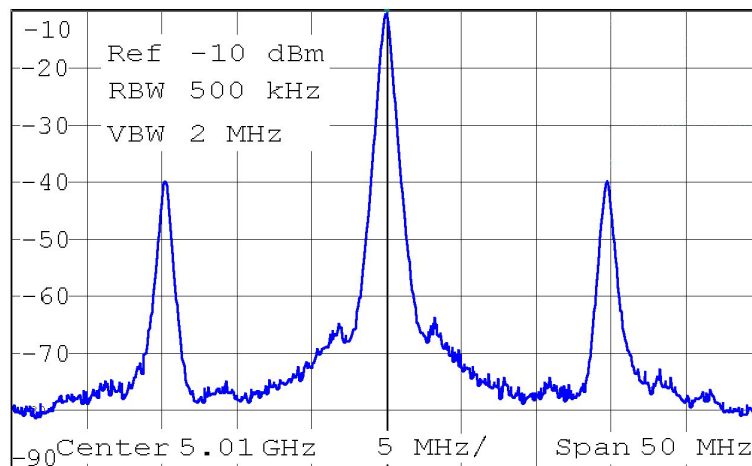


Figure 6.10. Output spectrum of the LC-VCO with an injected 5 GHz HFSN

### 6.3.1 Frequency offset

The frequency offset between the aggressor and the victim is a key parameter that affects the level of degradation of the LC-VCO. The model presented in chapter 5 showed a  $20 \text{ dB/dec}$  relationship between the frequency offset and the amplitude of the sidebands generated by the HFSN. In this particular design, this relationship has been used in order to make the oscillator very robust to the noise components around  $2.5 \text{ GHz}$ . An example of the output spectrum degradation of the LC-VCO due to HFSN has already been shown in Fig.6.10, where a  $10 \text{ dBm}$  noise tone was injected in the substrate with a frequency offset of  $15 \text{ MHz}$ . This high frequency noise generates two sidebands around the LC-VCO oscillation signal, exactly as shown back in chapter 4 and 5. The effect of the frequency offset on the  $5 \text{ GHz}$  LC-VCO has also been measured and it is shown in Fig.6.11. Fig.6.11 also shows the high accuracy of the model by comparing the measured relative amplitude of both sideband spurs against the amplitude predicted by the proposed model and against the exact numerical solution to the Adler's differential equation (5.30). The model shows a very high accuracy to predict the  $20 \text{ dB/dec}$  sideband amplitude decrease rate, except when the LC-VCO is about to lock, where the model prediction slightly differs from the measurements due to the very strong effect of pulling. Both the model and the mathematical solution fail to predict the behavior of the sideband at  $\omega_i$  for very high frequency offsets, where the amplitude saturates at a steady level. This effect is caused by the direct coupling of the HFSN to the output buffers, and so, not taken into account by the pulling models. According to the model, the expected relative level of the  $5 \text{ GHz}$  LC-VCO sidebands caused by HFSN at  $2.5 \text{ GHz}$  in this particular case is around  $-70 \text{ dB}$ , which, in most cases, should be almost imperceptible.

At this point, it has been proven that the  $5 \text{ GHz}$  LC-VCO performance is almost not affected by HFSN at  $2.5 \text{ GHz}$  but, can the HFSN at  $2.5 \text{ GHz}$  have a negative relevant effect on the frequency divider?. Fig.6.12 shows the measured output spectrum of one of the frequency divider outputs (driven by the output of the  $5 \text{ GHz}$  LC-VCO) when a  $10 \text{ dBm}$  noise tone is injected in the substrate with a frequency offset of  $3 \text{ MHz}$  with respect to the divider output frequency. Fig.6.12 shows that the frequency divider is very robust to that noise.

One issue observed in the measurement process is that the frequency divider modifies the occupied bandwidth of both, the carrier and the sidebands. As an example, Fig.6.13 shows the output spectrum of the  $5 \text{ GHz}$  LC-VCO and of the  $2.5 \text{ GHz}$  QVCO when affected by HFSN. This effect can be explained with the analysis of the LC-VCO bandwidth and the modulation frequency. As

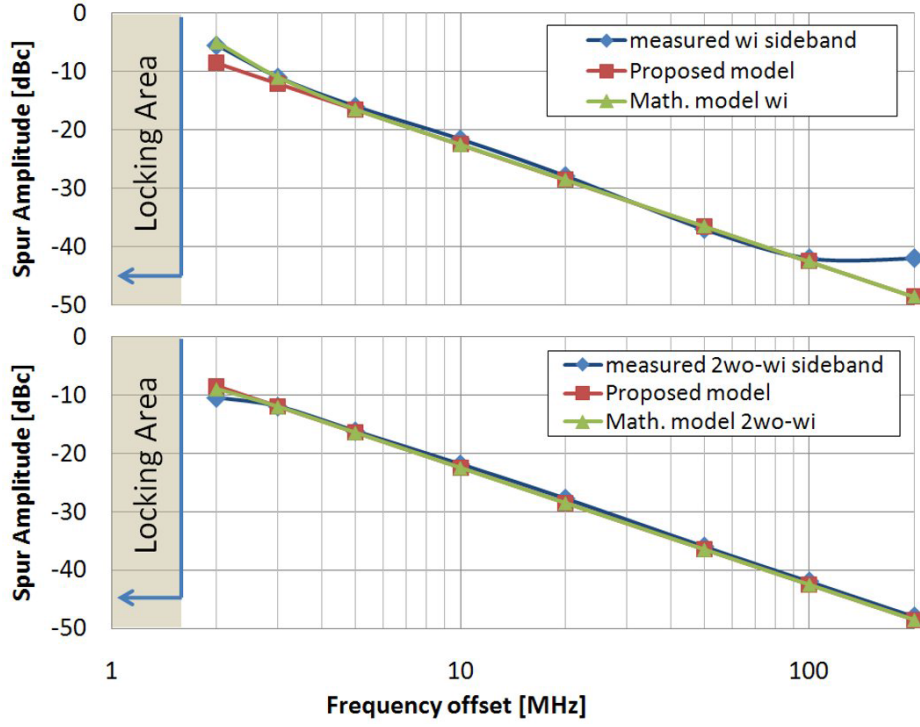


Figure 6.11. Measured relative amplitude of the sidebands on the LC-VCO due to injected 5 GHz HFSN

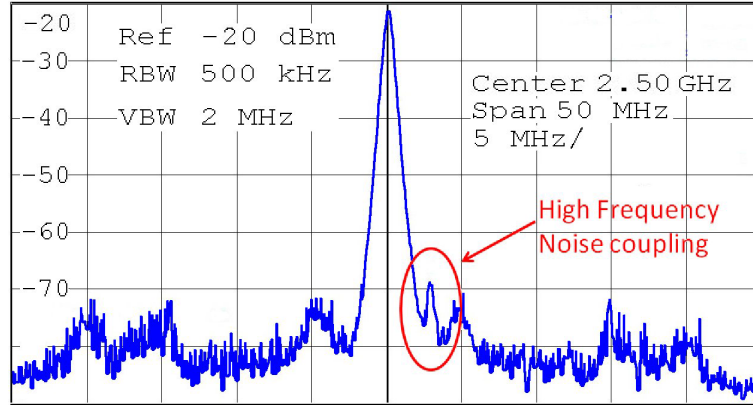


Figure 6.12. Effect of 2.5 GHz HFSN on the frequency divider

already explained, the modulation frequency is equal to the frequency offset between the instantaneous oscillation frequency and the frequency of the HFSN, so, the modulation frequency variation depends on the frequency stability of the LC-VCO, as shown in the following equation (6.3):

$$f_{mod} = f_c \pm \Delta f_c - f_n \quad (6.3)$$

where  $f_c$  is the central frequency of the LC-VCO,  $\Delta f_c$  is the variation of the LC-VCO around the center frequency and  $f_n$  is the frequency of the HFSN.

The frequency divider divides the instantaneous oscillation frequency by a factor of 2. So, the

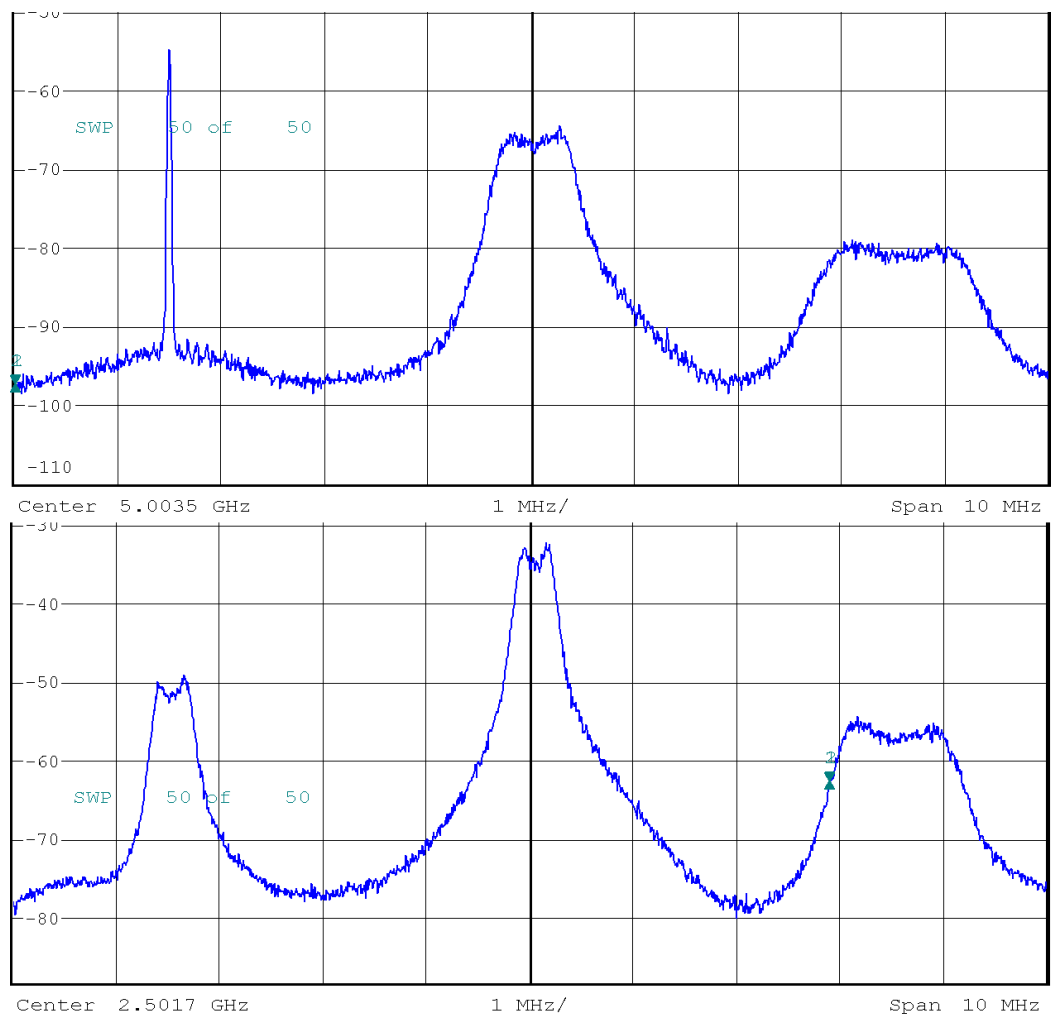


Figure 6.13. Occupied bandwidth of the carrier and the sidebands before and after the divider

central frequency and the variation of the frequency around it are also divided by 2. On the contrary, the modulation frequency is not affected by the divider. So, the instantaneous oscillation frequency after the divider is defined by:

$$f_d = f_c/2 \pm \Delta f_c/2 \quad (6.4)$$

The sidebands after the divider will fall around the divider oscillation frequency at a frequency offset equal to the modulation frequency. The bandwidth of each sideband will be determined by the maximum and the minimum frequency of the LC-VCO. The minimum frequency of the upper and lower sideband are determined by the minimum LC-VCO oscillation frequency. At that point, the modulation frequency is minimum. The maximum frequency of the upper and lower sideband are determined by the maximum LC-VCO oscillation frequency. At that point, the modulation frequency is maximum.

So, the frequency limits of the upper sidebands can be calculated as follows:

$$f_{uppersb\_min} = f_{d\_min} + f_{mod\_min} = (f_c/2 - \Delta f_c/2) + (f_c - \Delta f_c - f_n) = f_c/2 + (f_c - f_n) - \frac{3}{2}\Delta f_c \quad (6.5)$$

$$f_{uppersb\_max} = f_{d\_max} + f_{mod\_max} = (f_c/2 + \Delta f_c/2) + (f_c + \Delta f_c - f_n) = f_c/2 + (f_c - f_n) + \frac{3}{2}\Delta f_c \quad (6.6)$$

The subtraction of both terms, (6.6) and (6.5), shows the occupied bandwidth of the upper sideband.

$$f_{uppersb\_max} - f_{uppersb\_min} = 2 \cdot \frac{3}{2}\Delta f_c = 3\Delta f_c \quad (6.7)$$

The same analysis can be done for the lower sideband:

$$f_{lowersb\_min} = f_{d\_min} - f_{mod\_max} = (f_c/2 - \Delta f_c/2) - (f_c + \Delta f_c - f_n) = f_c/2 - (f_c - f_n) + \frac{1}{2}\Delta f_c \quad (6.8)$$

$$f_{lowersb\_max} = f_{d\_max} - f_{mod\_min} = (f_c/2 + \Delta f_c/2) - (f_c - \Delta f_c - f_n) = f_c/2 - (f_c - f_n) - \frac{1}{2}\Delta f_c \quad (6.9)$$

Again, the subtraction of both terms, (6.9) and (6.8), shows the occupied bandwidth of the lower sideband.

$$f_{lowersb\_max} - f_{lowersb\_min} = 2 \cdot \frac{1}{2}\Delta f_c = \Delta f_c \quad (6.10)$$

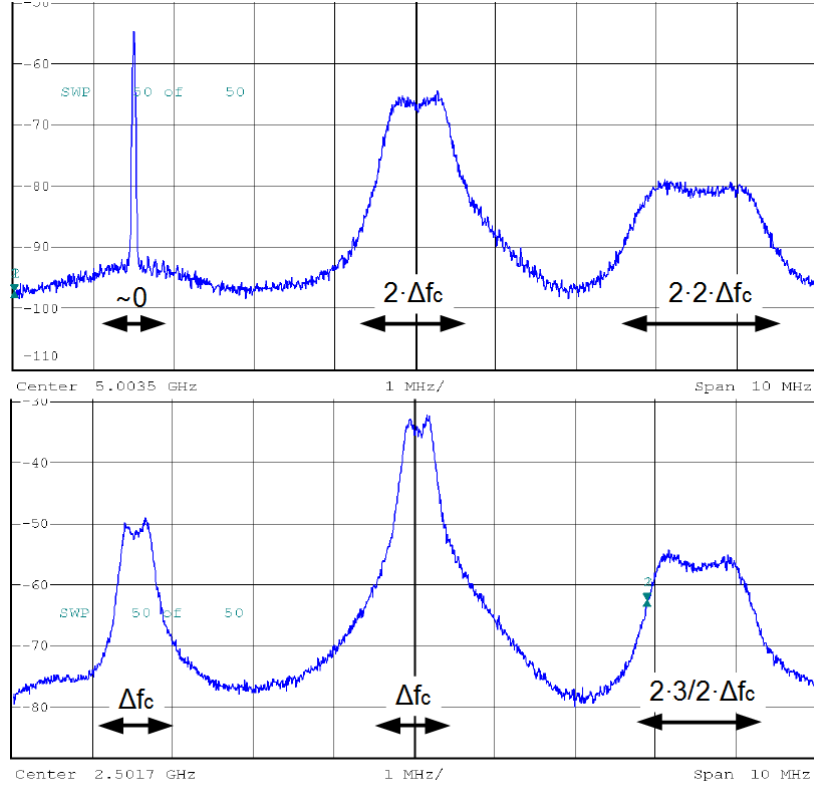


Figure 6.14. Calculated occupied bandwidth of the carrier and the sidebands before and after the divider

As a summary, the center frequency is divided from  $f_c$  down to  $f_c/2$ . The frequency offset between the center frequency and the sidebands is the same before and after the divider. The occupied bandwidth of the carrier signal is also divided by two, from  $2 \cdot \Delta f_c$  to  $\Delta f_c$ . The occupied bandwidth of the lower sideband (assuming that the HFSN is injected with a frequency lower than the carrier) goes from a very pure signal (very small occupied bandwidth) to  $\Delta f_c$ . The upper sideband changes from  $4\Delta f_c$  to  $3\Delta f_c$ . All this information is summarized in Fig.6.14. This analysis helps to understand the effect of the divider on the LC-VCO output but the presented changes on the sidebands do not have a relevant effect on the rest of the blocks after the divider.

### 6.3.2 Tank noise amplitude

The measures proposed back in Chapter 3 to reduce the noise coupling through the substrate have been applied in this design in order to reduce the amount of noise that reaches the LC-VCO. The main conclusions of chapter 3 state that guard rings connected to ground can be an efficient method to reduce the coupling between devices through the substrate. The efficiency of these guard rings highly depends on the quality of the current return path to ground. The impedance of the return

path should be minimized in order to effectively sink noise from the substrate. In this design, every single device, like transistors or passives, have been surrounded by a metal 1 ground ring connected to the substrate. This way, the guard rings reduce the noise coming through the substrate that can couple to the device as well as the amount of noise that the device itself injects into the substrate. The individual guard rings have been connected to a solid ground plane built with stacked Metal 1 and Metal 2 copper layers. The solid plane has a very low electric impedance and lets the return current to freely flow through the minimum length path. Metals 1 and 2 are the closest metal layers to the substrate, which increases the capacitive coupling between the substrate and the ground plane, providing a low impedance connection all along the ground plane to the high frequency components of the noise. Moreover, the high proximity between the metal plane and the substrate reduces the effective area of the return current loop, reducing its effective inductance, and so, its high frequency impedance.

Finally, the DC power supplies can easily couple noise to the tank. Noise decoupling capacitors have been included in the design both at chip level and at PCB level, granting a low impedance in a very wide range of frequencies for all the dc lines.

### 6.3.3 Tank quality factor

Back in section 5.2.2, a mathematical description of the tank quality factor concept was presented. From a more intuitive point of view, the tank quality factor represents a quantitative approach to “how close is the tank to an ideal tank”, understanding the concept of *ideal tank* as that built with ideal passive L-C components. An ideal tank is completely lossless and would have an infinite quality factor, but actual implementations have losses that degrade Q and deviate the tank behavior from ideality. At RF frequencies, inductors are usually the main source of energy loss.<sup>2</sup> The most obvious source of inductor losses is the series winding resistance. Using thick and wide track to build the inductor can reduce the series resistance but CMOS processes only allow to use relatively thin and narrow tracks, limiting the effectiveness of this measure. Eddy currents is another source of resistive loss. They cause a nonuniform current distribution along the section of conductors, pushing current to the outer skin of the conductors (skin effect) and, so, reducing the effective section of the conductor. Eddy currents are stronger in the inner turns of the spiral inductor where the created magnetic field is stronger [129]. Inductor layout with non-uniform metal width and non-uniform metal

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<sup>2</sup>Chapter 7 will show that, at millimeter wave frequencies, capacitors and varactor may also become a very relevant source of losses.



spacing has proven to reduce the effect of Eddy currents [120]. Another important source of losses in CMOS processes is the energy lost into the substrate. Due to proximity between the inductor and the substrate, a parasitic capacitance is created between them. The resistive substrate is then seen as a resistor in series with the parasitic capacitance. High frequency currents can flow into the substrate through this capacitance. In order to reduce this effect, higher metal levels are usually used in the inductor construction. Lowering the inductor track width also helps but it is at the price of increasing the track series resistance. The magnetic field created by the inductor is a third source of losses. The magnetic field penetrates into the substrate and creates image currents (parallel current in the substrate with opposite direction). These currents are converted to heat by the resistive substrate. Patterned ground shields (introduced in chapter 2 and widely discussed in chapter 7) have proven to be a very effective measure to prevent these currents. Fig. 6.15 shows a typical real inductor model including all the sources of losses discussed in this section.  $L$  and  $R$  represent the inductance and series resistance of the inductor respectively.  $C_{ox}$  stands for the dielectric layer capacitance and  $C_{sub}$  and  $R_{sub}$  model the P substrate.  $C_F$  represents the capacitance between the different inductor windings. Finally,  $R_{sub(m)}$  and the transformer model the mirror currents induced in the substrate.

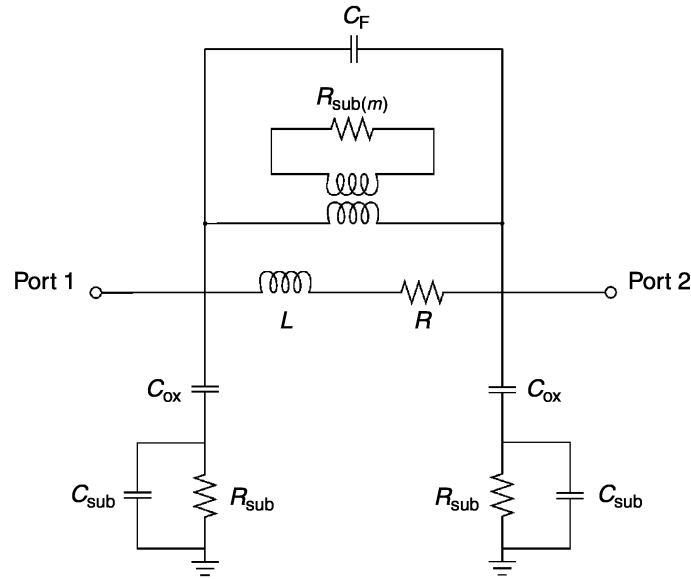


Figure 6.15. Generic model of a real CMOS inductor [130]

According to the proposed model, the tank quality factor ( $Q$ ) of the LC-VCO should be maximized in order to increase the immunity to HFSN. Maximizing  $Q$  will also positively impact other characteristics of the circuit like power consumption, output power or phase noise. The inductor Quality factor maximization in our  $5\text{ GHz}$  LC-VCO has been achieved by using a  $4.5\text{ }\mu\text{m}$  thick

metal layer, which minimizes the series resistance, together with a non-constant track width design that optimizes the  $Q$  value at high frequencies [120]. A P+ substrate guard ring has been added in order to increase the isolation of the inductor to substrate noise and to limit the proximity effects of neighboring components on the inductance value [131]. An important trade off appears here since a guard ring within short distance of the inductor can severely degrade its quality factor at high frequencies [131], reducing its robustness against high frequency substrate noise. The distance between the inductor and the guard ring can be increased in order to reduce the negative effect on the  $Q$  but it would, consequently, increase the required area for the inductor. Several simulations were carried out in order to find the best distance between the inductor external edge and the guard ring, optimizing the trade off between robustness,  $Q$  and area. Fig.6.4 shows the layout of the inductor implemented together with its measured inductance and quality factor.

#### 6.3.4 Oscillation amplitude

In order to increase the robustness of the LC-VCO to HFSN the oscillation amplitude should be maximized. The optimization process of the tank quality factor has already had a positive impact on the oscillation amplitude. As it has been explained in section 5.2.2, the amplitude of the oscillation depends on the loss of energy in the tank, which depends on the tank quality factor. Consequently, the maximization of the tank quality factor presents a double effect on the robustness of the LC-VCO to HFSN, due to the  $Q$  itself and due to the effect on the amplitude. A second design decision to maximize the oscillation amplitude is to use a CMOS configuration, which provides 6dB of increased amplitude compared to a NMOS or PMOS only configuration [86], [132] without increasing the power consumption. Finally, the oscillation amplitude can be increased by increasing the biasing current, which in our design can be controlled using the voltage level at the tail transistor gate *NM3*. Fig.6.16 shows the relationship between the *NM3* gate voltage, the biasing current and the LC oscillator amplitude. As expected, the oscillation amplitude grows with the power consumption. At the same time, as predicted by the proposed model (5.53), the relative sideband amplitude decreases when the oscillation amplitude increases. Fig.6.17 shows this effect. Consequently, a designer has the possibility to increase the robustness of the LC-VCO to HFSN increasing the oscillation amplitude by investing in power consumption. Nevertheless, in this particular oscillator - divider structure, the output of the divider presents a very low sensitivity to the input amplitude (ie, the LC-VCO oscillator amplitude) due to the amplitude limiting factor of the CML latches. Consequently, the change

on the 5 GHz LC-VCO oscillation amplitude has a very small effect on the 2.5 GHz output, having a very weak impact on the performance of the rest of the system.

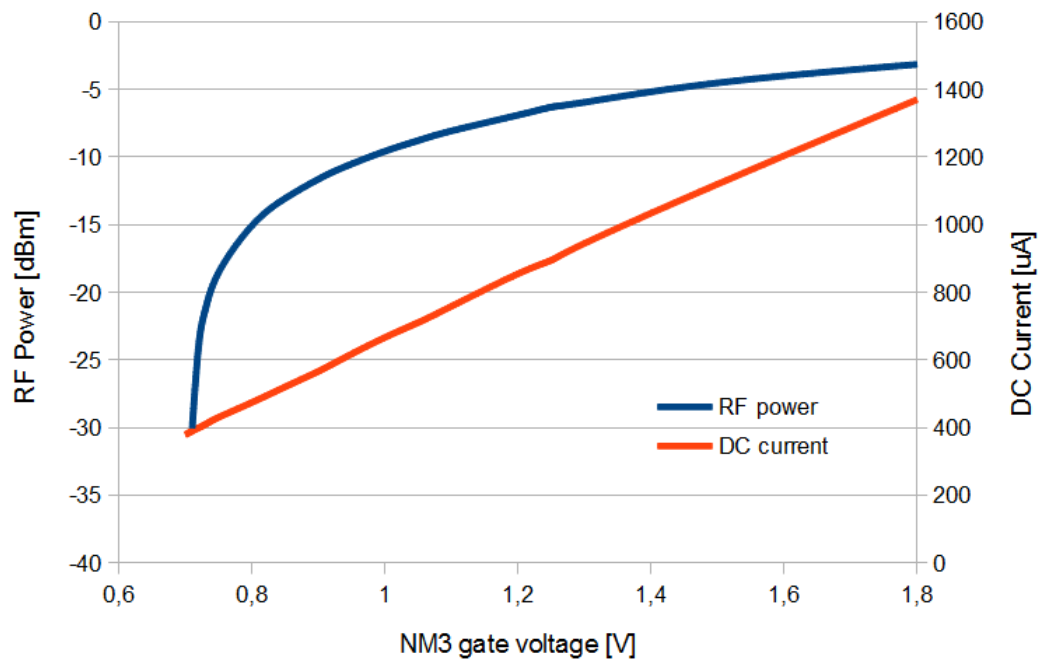


Figure 6.16. Relationship between the NM3 gate voltage, the biasing current and the LC oscillator amplitude.

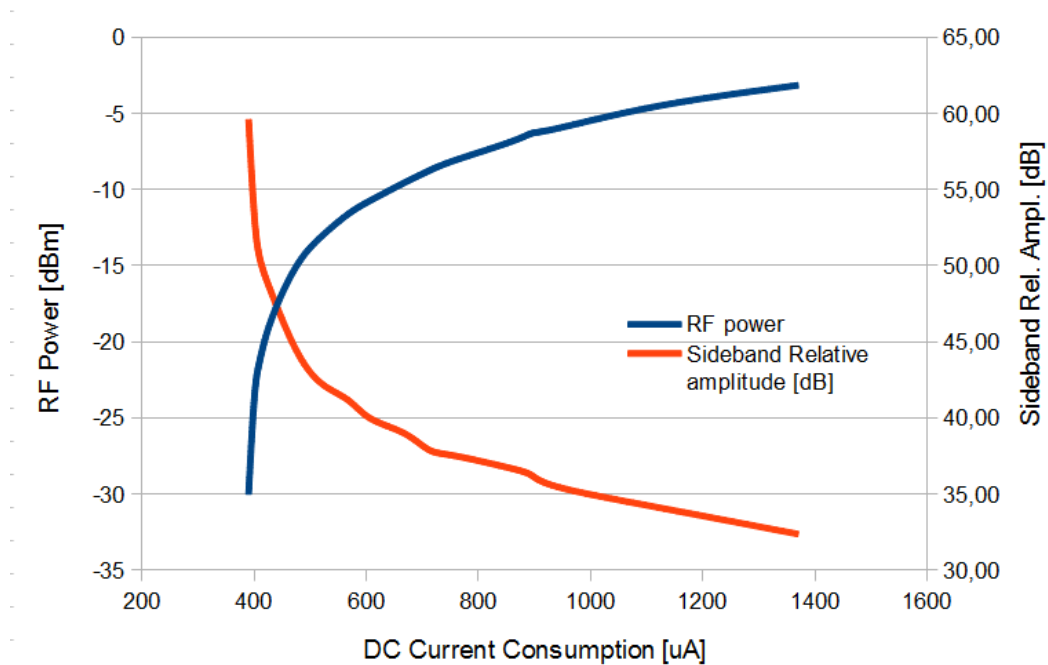


Figure 6.17. LC oscillator amplitude and sideband amplitude for different biasing current values.

### 6.3.5 Oscillation Frequency

The proposed model states that the higher the oscillation frequency the higher the sensitivity of the LC-VCO to HFSN. This fact counts against the proposed strategy as doubling the oscillation frequency would double the performance degradation of the oscillator. Consequently, a  $5\text{ GHz}$  LC-VCO is more sensitive to HFSN than a  $2.5\text{ GHz}$  LC-VCO. The analysis of the effect of dividing the instantaneous frequency of a frequency modulated signal shows that this effect is compensated by the frequency divider. Fig.6.18 shows the output spectrum of a frequency modulated signal before and after a  $\div 2$  frequency divider. As stated back in chapter 4, the output spectrum of a frequency modulated signal is determined by the signal amplitude (which determines the carrier amplitude), the modulation frequency (which determines the frequency offset and the relative amplitude of the sidebands) and the maximum frequency deviation (which determines the relative amplitude of the sidebands). The effect of the frequency divider on each of these parameters will define the output spectrum after the divider.

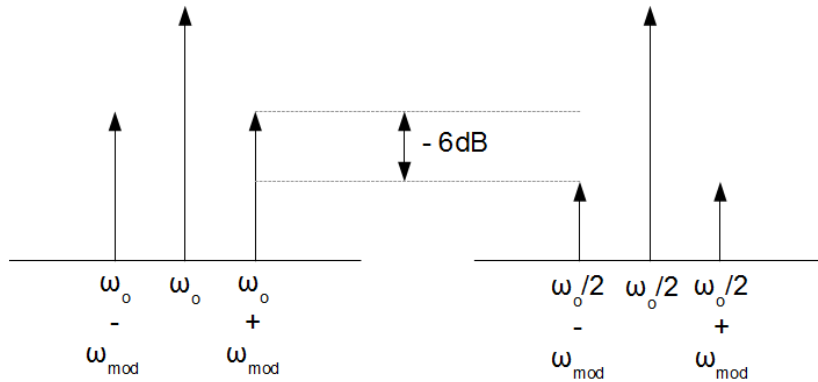


Figure 6.18. Spectrum of a frequency modulated signal (left) and of the same modulated signal after a times 2 frequency divider (right).

- Carrier amplitude: Back in section 6.2, it has been shown that the output amplitude of the frequency divider depends more on its design than on the input signal. So, the amplitude of the carrier on the output spectrum will be quite independent of the input carrier amplitude.
- Sideband frequency offset: The offset between the carrier and the generated sidebands is determined by the modulation frequency. The effect on the modulation frequency of a frequency divider can be easily understood if it is analyzed from a time domain perspective. In a frequency modulation signal the frequency increases and decreases periodically. The time between two instants of maximum frequency defines the modulation period, and so, the modulation fre-

quency. The frequency divider divides the frequency by a factor of 2, and so, the output frequency is maximum (or minimum) at the same time than in the input signal. Consequently, the modulation frequency of the frequency divided signal is the same as that of the original signal. The frequency offset of the sidebands is exactly the same in both the input and the output signals of the frequency divider.

- Sideband relative amplitude: The relative amplitude of sidebands in a frequency modulated signal depends on two factors: the modulation frequency and the maximum frequency deviation. In the case of the frequency divider, it has been shown that the modulation frequency does not change, so, the relationship between the input and output relative sideband amplitudes only depends on the maximum frequency deviation. As the frequency divider divides the instantaneous frequency by a factor of 2, it is easy to deduce that the maximum frequency deviation is also divided by 2. As a representative example, if the input signal oscillates at a center frequency of 5 GHz with a maximum deviation of 0.1 GHz (ranging 4.9 GHz-5.1 GHz) the output signal will oscillate at a center frequency of 2.5 GHz with a maximum deviation of 0.05 GHz (ranging 2.45 GHz-2.55 GHz). As the sideband amplitude is proportional to the maximum frequency deviation (see 5.4.1), the  $\div 2$  frequency dividing factor translates into a 6 dB amplitude reduction. This effect is shown in Fig.6.19 and Fig.6.20. They show the effect on the LC-VCO and on the QVCO of a 10 dBm noise signal injected in the substrate at an offset frequency of 4 MHz. Fig.6.19 shows the output spectrum of the 5 GHz LC-VCO. Fig.6.20 shows the output spectrum of the frequency divider. The comparison between the sidebands on both figures shows that the frequency divider provides approximately 6 dB of relative amplitude reduction (actually  $(-22.19 \text{ dBm}) - (-28.64 \text{ dBm}) = 6.45 \text{ dB}$ ). Note that, due to the inaccessibility of the LC-VCO output, the 5 GHz signal has been measured at the output of the complete system (after the output buffer), where the 5 GHz signal arrives through coupling, explaining the highly reduced carrier amplitude.

## 6.4 Summary and conclusions

This chapter has presented the first of two scenarios where the capabilities of the model have been evaluated to prove its high utility as a design tool to reduce the effect of HFSN on an LC-VCO. Following the guidelines provided by the model, a HFSN robust QVCO has been designed

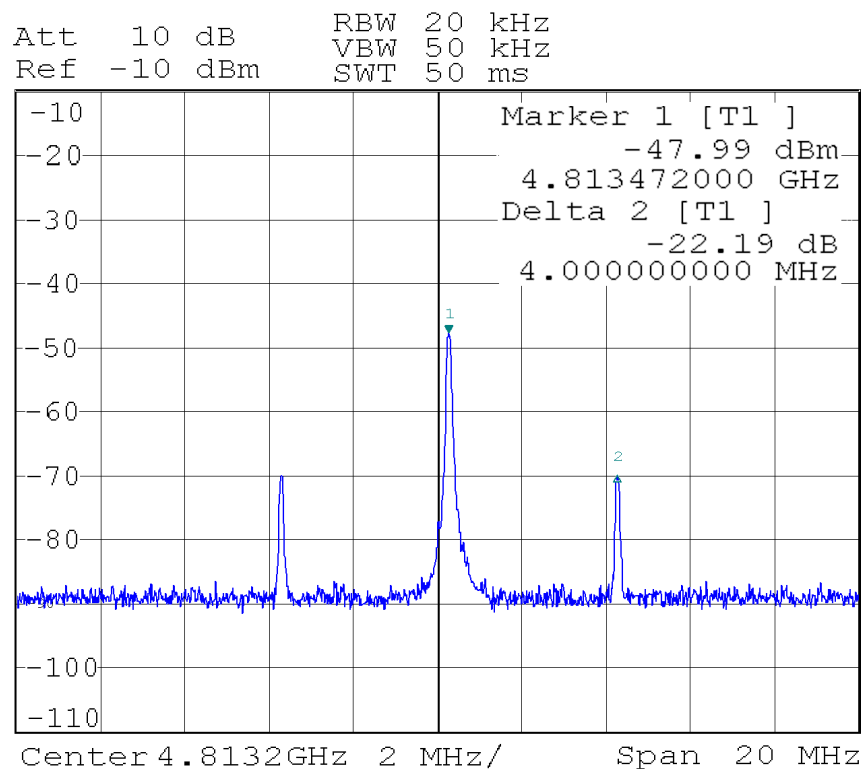


Figure 6.19. Output spectrum of the 5 GHz LC-VCO affected by HFSN

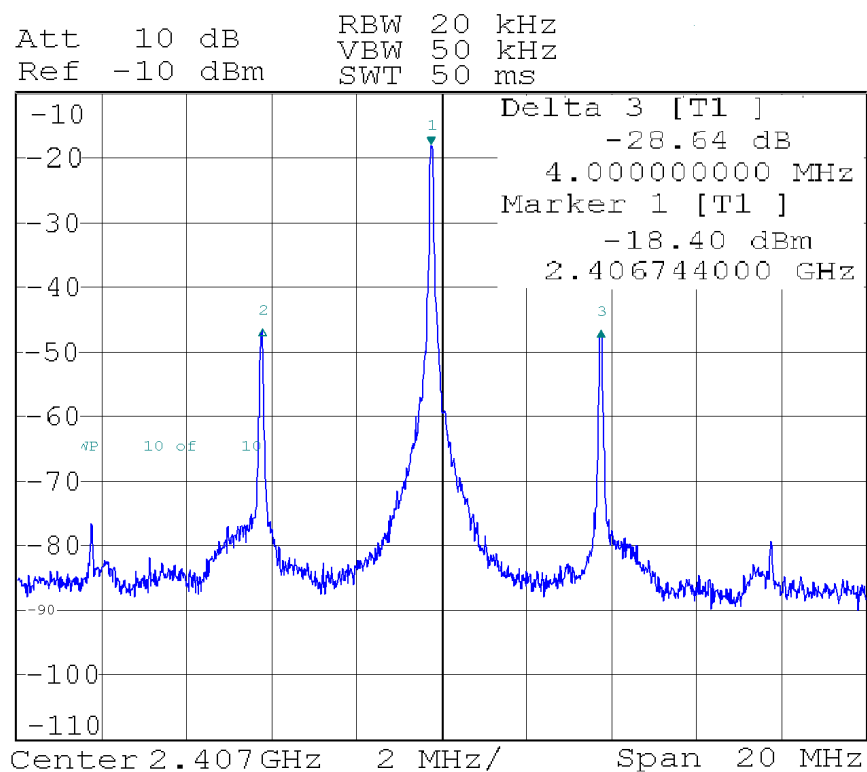


Figure 6.20. Output spectrum of the 2.5 GHz QVCO affected by HFSN

with characteristics suitable to the main 2.5 GHz ISM band wireless communication standards like Bluetooth, WiFi or ZigBee.

A common technique in transceivers design to protect the oscillator from the noise of the rest of the blocks is the use of a frequency divider. In this case, the LC-VCO oscillates at double of the transceiver working frequency and then it is divided by two. The frequency divider also generates the I and Q components.

The model states that the frequency offset between the LC-VCO oscillation frequency and the frequency of the substrate noise is a key parameter that determines the robustness to HFSN. The designed QVCO has shown to be immune to the HFSN around 2.5 GHz, where most of the rest of subsystems of the transceiver work (and generate noise). Thanks to the big offset with the oscillation frequency of the  $5\text{ GHz}$  LC-VCO, the pulling effect on the oscillator is extremely small. Some measures have also been taken to maximize the robustness to HFSN around the LC-VCO oscillation frequency, 5 GHz, where, according to the model, the oscillator is more sensitive to HFSN. These measures deduced from the model have proven to be effective to reduce the effect of HFSN while showing very small negative impact on the optimal performance of the QVCO. This investigation has empirically proven the validity and accuracy of the model and its usefulness to design a HSFN robust 2.5 GHz QVCO.





## Chapter 7

# Analysis of the HFSN effect on millimeter wave LC-VCOs.

### 7.1 Introduction

Previous chapters have already shown that the integration of an LC-VCO with the rest of the blocks of an RF or mixed signal system in a common substrate can be highly limited by their mutual interactions. It is expected that HFSN problems will worsen as the technology scales and frequencies used in communication circuits exceed the RF range, entering the mm wave range (mmW). As it was already discussed in chapter 3, capacitive coupling gains relevance and noise transmission through the substrate is easier due to the lower impedance of silicon substrate at those frequencies [7]. Moreover, most of the typical measures to isolate the sensitive blocks from HFSN lose their efficacy or are difficult to implement in the mmW band. For example, the isolation provided by protection structures, such as guard rings or wells, is reduced as the frequency increases beyond the RF range due to the difficulty of sinking noise to a clean ground [8], [9]. Very little work has been done on the robustness to HFSN of LC-VCOs oscillating in the mmW band or about the efficiency of shielding techniques in this frequency range.

This chapter analyzes the impact of high-frequency substrate noise on two 60 *GHz* LC-VCOs that implement different strategies for inductor shielding, namely floating and grounded shields. These oscillators are presented in section 7.2. The analytical model proposed back in chapter 5 is used in section 7.3 to identify the circuit parameters that determine the level of the sidebands

created by the noise. These parameters are individually evaluated for the two LC-VCOs in section 7.4, identifying their relative responsibility for the observed noise effects. The predictions of the analytical model and the conclusions obtained are finally validated by comparing against detailed simulations of HFSN impact on the LC-VCOs in section 7.5, and against experimental measurements in section 7.6. The analysis provides a very relevant conclusion: the floating inductor shield provides extra immunity to HFSN compared to the grounded inductor shield, and this advantage is essentially due to the improvement in the tank quality factor and not due to a better isolation from the substrate.

## 7.2 mmW VCOs Description

Two different 60  $GHz$  LC-VCOs for a wireless HDMI receiver have been designed and fabricated in a 65  $nm$  bulk CMOS process. Both VCOs are identical except for the tank inductor design, where two different inductor shielding strategies have been used. In one case, the inductor shield has been connected to the common ground (grounded shield inductor VCO) while, in the other case, it has been left unconnected (floating shield inductor VCO).

### 7.2.1 Inductor description

The inductors have been fabricated in a 65  $nm$  bulk CMOS process with 1 poly and 6 copper metal layers, being the top layer a thick metal. Both inductors are single turn differential inductors of, approximately, 95  $pH$  DC inductance. The grounded shield inductor has been designed with a patterned ground shield made of polysilicon and diffusion, connected to ground through stacked M1 and M2 forming an X-shape (see Fig. 7.1 left). The floating shield inductor has been protected using an orthogonal pattern of floating metal lines laid in M1 and M2 (see Fig. 7.1 right).

Floating shields have been proposed as a better performance and reduced loss alternative to grounded shields [69]. In a symmetric differential inductor with a symmetric patterned floating metal shield, the center of the shield (and i.e. the center of the inductor) can be treated as a virtual ground. This virtual ground reduces the RF currents in the shield reducing the amount of energy loss in the substrate. The isolation between different devices is also improved with the use of floating shields.

The two inductors used in the VCOs were fabricated in individual test structures in order to characterize their inductance and quality factor, after an accurate de-embedding of the effects of pads

and interconnects. Measurement results agreed with EM simulations of the inductors using Agilent Momentum simulator. Table 7.1 summarizes the results obtained at the central frequency of both VCOs [133]. The floating shield inductor shows a slight increase in the inductance ( $5\text{ pH}$ ), but most important a 50% improvement in the quality factor.

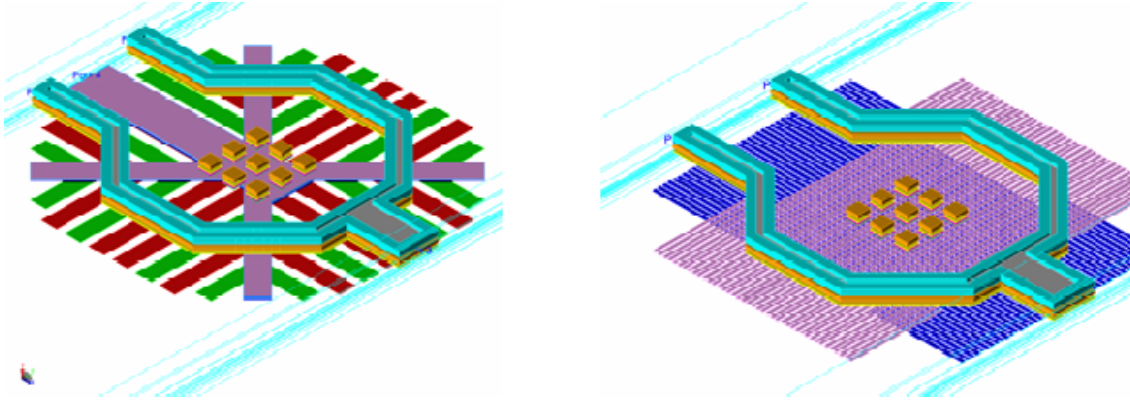


Figure 7.1. Layouts of the grounded shield (left) and floating shield (right) inductors

	Grounded Shield	Floating Shield
L@55 GHz	89 pH	94 pH
Q@55 GHz	18	27

Table 7.1. Inductors Characteristics

The isolation between the substrate and the inductor provided by both shielding strategies has also been analyzed through EM simulations. A substrate contact has been added near the inductors, and isolation has been evaluated in terms of S12 parameter. Simulations have shown that the floating shield outperforms the grounded shield when the noise signal is injected in the inductor symmetry axis and very close (tenths of microns) to the inductor. But as soon as the injection point is moved further away from the inductor or displaced from the symmetry axis, both shields provide very similar isolation. Thus this is the expected behavior in the general case of distributed substrate noise with random origin. Fig. 7.2 shows the simulated isolation between the substrate injection pad and the differential inductor, showing negligible differences at the frequencies of interest.

## 7.2.2 mmW VCOs characteristics

Both  $60\text{ GHz}$  LC-VCOs were designed using a cross-coupled differential NMOS topology and a PMOS DC tail current supply. The LC tank was built with the inductors described before, a contin-

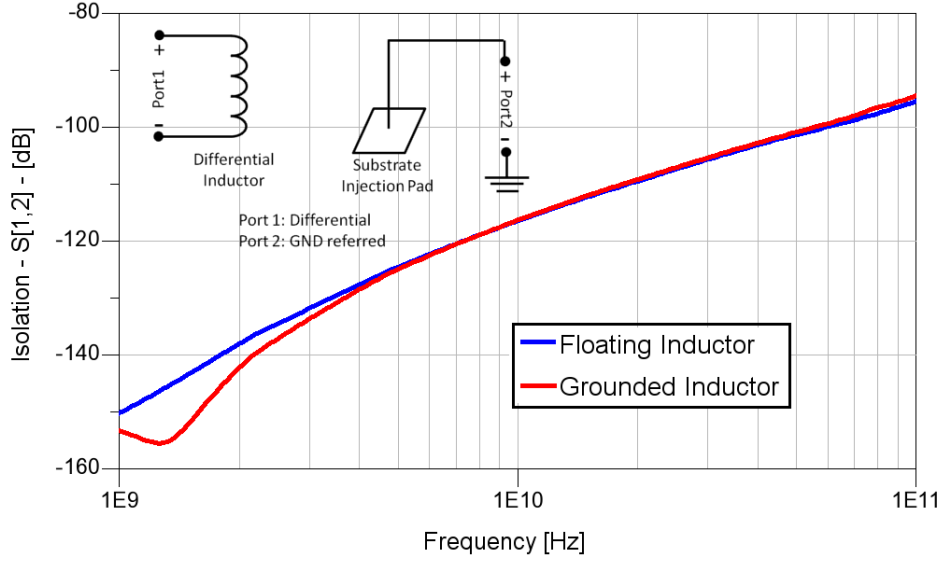


Figure 7.2. Simulated isolation between the substrate and the inductors.

uously controlled differential varactor, and a bank of digitally controlled switching capacitors. Two output buffers were included in the design in order to drive the  $50\ \Omega$  loads. A microphotograph of the fabricated chip and a simplified schematic of the VCO are shown in Fig. 7.3. Both versions of the VCO are identical except for the inductors, and have been measured in the same conditions, consuming  $15\text{ mW}$  from a  $1.2\text{ V}$  supply, and showing an outstanding tuning range. The measured performance of both VCOs is summarized in Table 7.2. A detailed description of the design process and extensive information about VCO modeling, simulation results, and measurements can be found in [134].

	Grounded Shield VCO	Floating Shield VCO
Technology	CMOS 65 nm	CMOS 65 nm
Supply voltage	1.2 V	1.2 V
Power Consumption	15 mW	15 mW
Osc. Freq	51–61 GHz	49.5–59 GHz
Freq. Tuning Range	17%	17%
Osc. ampl @ 15 mW	-9 dBm	-7 dBm

Table 7.2. VCO Characteristics

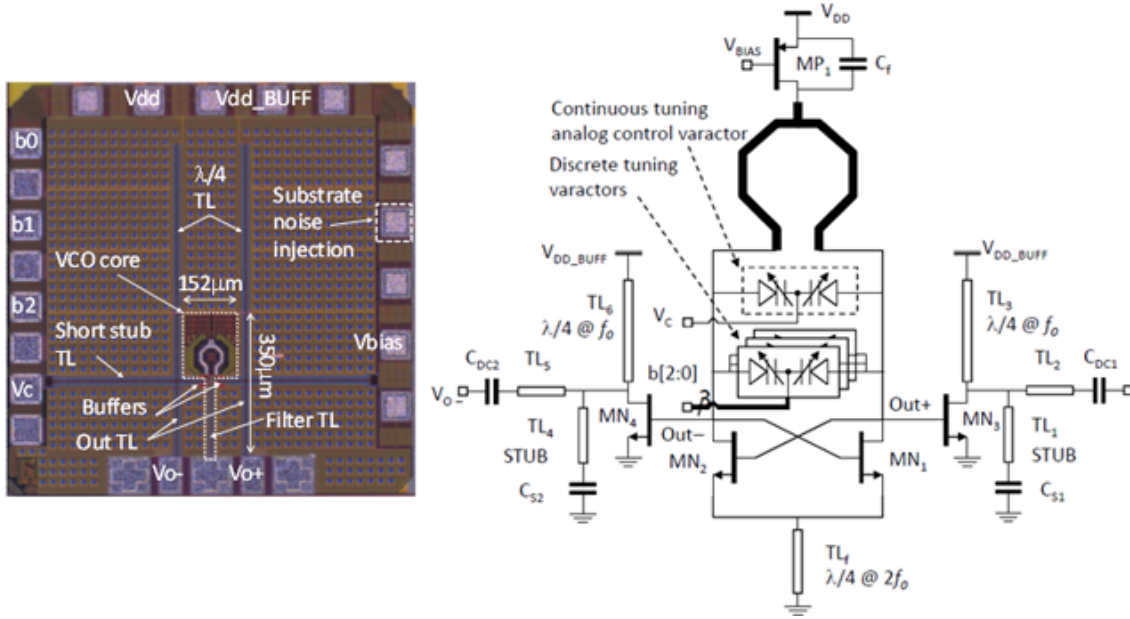


Figure 7.3. Test chip microphotograph and simplified schematic.

### 7.3 Simulation of HFSN effect on the LC-VCO

The effect of HFSN on both VCOs has been simulated in order to observe the difference in VCO performance caused by the different shielding strategies of the inductors. The coupling of HFSN from the substrate has been modeled as a single tone voltage source connected in series with the tank inductor. This source is identical for both VCOs, which means that we have initially assumed that the substrate noise reaching the tank of the two VCOs is the same. This assumption is based on several reasons. Firstly, the results of the isolation simulations in section 7.2.1 show a very similar performance for both inductors. Secondly, the inductor is not necessarily the dominant coupling path between the substrate and the tank [10], [47]. There are multiple points of connection between the substrate and the circuit ground, which are identical on both VCOs, that can pick up noise from the substrate and cause the circuit ground to bounce. Ground bounce can easily reach the tank through power lines or transistor bulk connections. The high isolation between the inductor and the substrate achieved by both shielding structures makes this scenario very feasible. The experimental measurements in section 7.5 will show that using the same noise voltage source on both VCOs is a valid assumption.

A transient analysis was performed in order to observe the VCO output degradation caused by the HFSN. Fig. 7.4 shows the simulated instantaneous oscillation frequency and the output spectrum of the VCO when the tank is affected by a  $10\text{ mV}$  tone with a frequency offset of  $\Delta f = 0.8\text{ GHz}$ .

respect to the VCO output  $f_o$ . The noise tone modifies the instantaneous frequency of the oscillator resulting in a frequency modulation of the VCO output where the modulation frequency is equal to the offset frequency  $\Delta f$ . Consequently, the perturbed spectrum of the VCO output shows two symmetrical sidebands around the oscillation frequency at  $f_o + \Delta f$  and  $f_o - \Delta f$ . This simulation has been repeated for different values of the control voltage,  $V_c$ , on both VCOs, and the results obtained are shown in Fig. 7.5. The amplitude of the sideband spurs has a strong dependence on  $V_c$ . The immunity of both VCOs to HFSN is very similar for low values of  $V_c$ . As  $V_c$  increases, the robustness of both VCOs increases but the improvement rate is higher in the floating shield inductor VCO. Thus, for high values of  $V_c$  the floating shield inductor provides better noise immunity than the grounded shield inductor.

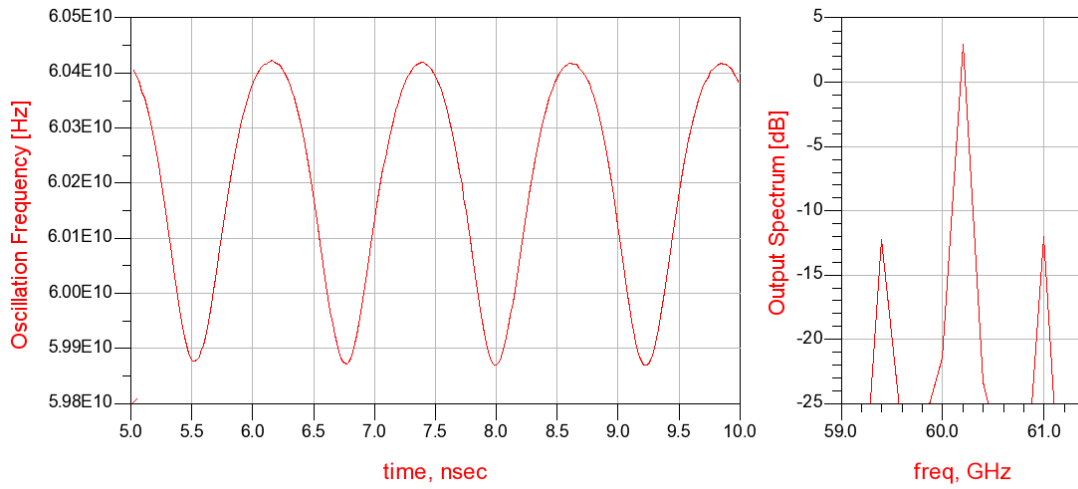


Figure 7.4. Effect of HFSN on the instantaneous oscillation frequency and output spectrum.

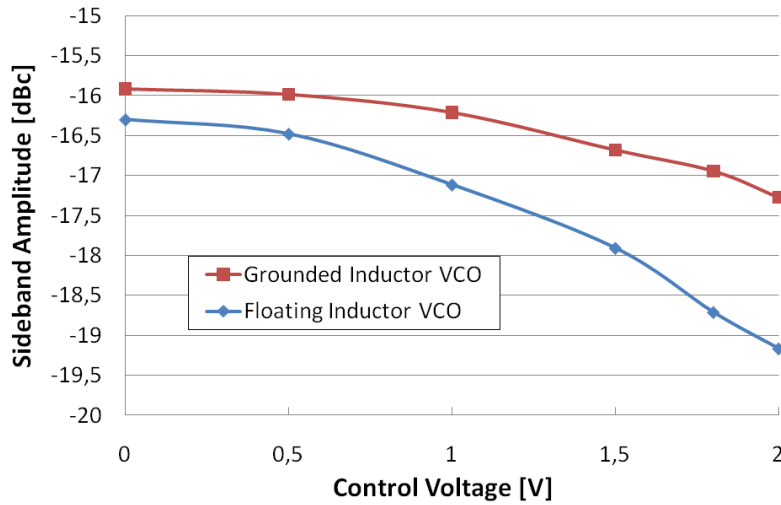


Figure 7.5. Relationship between  $V_c$  and the sideband spur amplitude caused by HFSN on both VCOs.

The relationship between the VCO biasing current and the amplitude of the sidebands has also been simulated, and the results are shown in Fig. 7.6. Note that a decrease in bias voltage produces an increase in current consumption. Thus Fig. 7.6 shows how an increase in the power consumption of the VCO reduces the maximum frequency deviation caused by the HFSN, and thus the amplitude of the sidebands, therefore improving the robustness to HFSN.

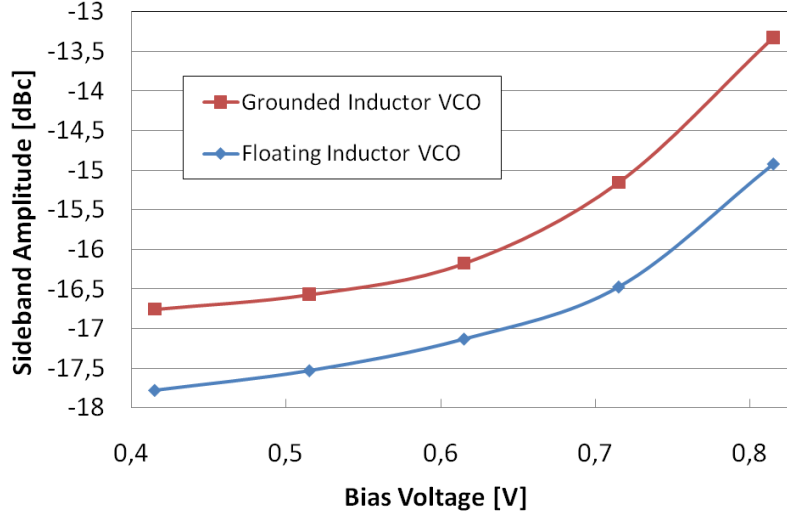


Figure 7.6. Relationship between  $V_{bias}$  and the sidebands' relative amplitude caused by HFSN in both VCOs.

The results of these simulations show that, even assuming that the amount of noise reaching the tank from the substrate is the same for both VCOs, they have different levels of robustness to HFSN. The level of the sideband spurs on both VCOs is highly dependent on some controls of the VCO, such as the biasing current or the control voltage. The cause of these dependencies can be understood with the help of the mathematical model proposed in chapter 5. Next section relates the differences observed to the two inductor shielding strategies.

## 7.4 Analysis of the contributors to VCO performance degradation

The analytical model, (5.48), will be used in this section to identify the parameters responsible for the noise behavior observed in the simulations of section 7.3, and most particularly their relationship with the two inductor shielding strategies. Specifically, the differences in tank quality factor  $Q$ , VCO output amplitude  $A_o$ , and oscillation frequency  $\omega_o$  will be individually evaluated by means of simulations. The models of the inductors are obtained from EM simulations using Momentum from Agilent Technologies [29], while the models provided by the manufacturer in the design kit were used

for the varactor and switch capacitances. The interconnect lines between the different components of the tank have also been modeled with Momentum and included in the tank simulation, while the possible degradation of the tank  $Q$  due to the parasitics of the active elements was ignored. This modeling approach of the tank was also used in simulations of the complete VCO, together with the transistor models provided in the design kit.

#### 7.4.1 Analysis of the tank quality factor

The quality factor of an LC tank VCO is mainly dominated by the quality of the tank passives. A commonly used expression to approximate the tank  $Q$  from its passives'  $Q$  is (7.1) [135].

$$\frac{1}{Q_{Tank}} = \frac{1}{Q_L} + \frac{1}{Q_C} \quad (7.1)$$

where  $Q_L$  and  $Q_C$  are the quality factors of the inductor and capacitors—including varactors—respectively.

It is well known that at low RF frequencies, the tank  $Q$  is dominated by the inductor, while at mmW frequencies, the  $Q$  of the varactor decreases and becomes comparable or even dominates the inductor  $Q$ . Fig. 7.7 shows the simulated varactor capacitance and  $Q$  at  $60\text{ GHz}$  as a function of the control voltage,  $V_c$ . It can be checked that the  $Q$  values obtained are comparable to those of the inductors shown in Table I. This, together with the strong dependence of the varactor behavior on the value of  $V_c$ , makes the control voltage a very important parameter in the analysis of the tank  $Q$ . For low values of  $V_c$ , the varactor  $Q$  is well below that of the inductors, dominating the tank  $Q$ . Consequently, a small difference is expected between the  $Q$  of both VCO tanks for low values of  $V_c$ . As  $V_c$  increases, the  $Q$  of the varactor grows drastically. Then the values of the inductor and varactor  $Q$  become similar, both of them have comparable contribution to the tank  $Q$ , and therefore the difference between the  $Q$ 's of the inductors becomes relevant. In summary, this qualitative first approach predicts the tank  $Q$  of the floating inductor VCO will show better values than the grounded inductor VCO but only for high values of  $V_c$ . In order to confirm this behavior, both VCO tanks have been accurately simulated. The results of the tank quality factor of both VCOs are shown in Fig. 7.8, and fully confirm the conclusions derived from the qualitative discussion.



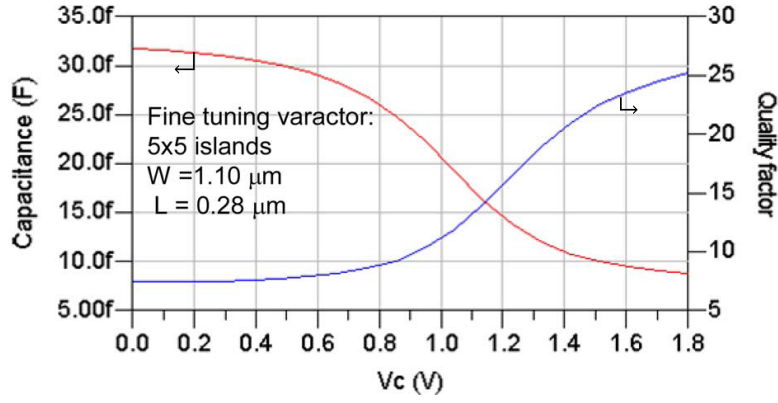


Figure 7.7. Varactor capacitance and quality factor as functions of the control voltage  $V_c$ .

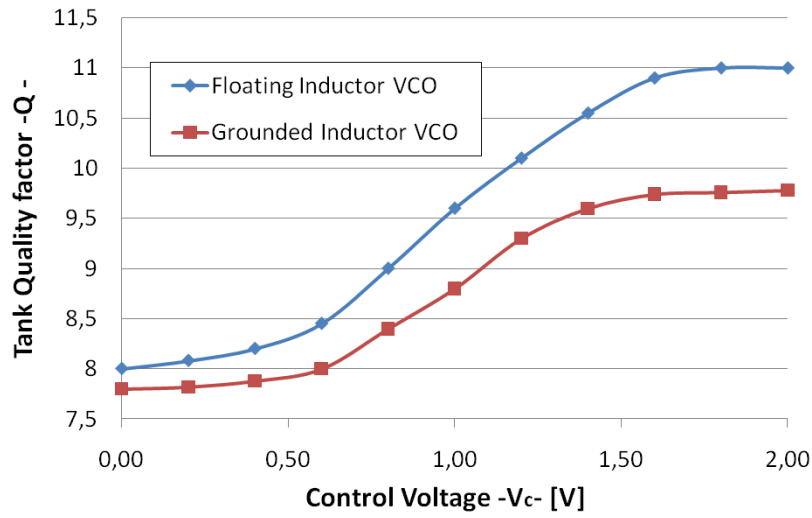


Figure 7.8. Tank quality factor of the grounded and floating VCOs.

## 7.4.2 Analysis of the oscillation amplitude

Expression (5.48) shows that the bigger the oscillation amplitude, the better the robustness to HFSN. It is well known that the oscillation amplitude of a VCO is directly related to its tank  $Q$ . Therefore, a strong correlation is expected between the results obtained in the tank  $Q$  analysis and the oscillation amplitude behavior. This is confirmed in Fig. 7.9, which shows the oscillation amplitude obtained from simulations of both VCOs for different values of the control voltage. Both VCOs have very close behavior for low values of  $V_c$ , but as this control voltage is increased, the amplitude of the floating inductor VCO grows at a faster rate than the grounded inductor VCO amplitude, following the expected correlation with the tank  $Q$ . Fig. 7.10 also shows how the power consumption can be selected with  $V_{bias}$  but is the same for both VCOs, therefore the differences in the oscillation amplitude cannot be attributed to differences in power consumption.

If we now state that an improvement in the tank  $Q$  allows an increase in the oscillator amplitude and this produces an improvement in the robustness of the VCO against high frequency added noise, it can be regarded as something well known or even obvious. But if we look at (5.53) we can see that an improvement in the tank  $Q$  produces a double advantage in terms of HFSN reduction: as we have already said, first by increasing  $A_o$ , but also by the  $Q$  improvement itself. In other words, we can decrease the power consumption of the highest  $Q$  VCO—floating shield—so that both VCOs have the same output amplitude  $A_o$ , but even then the floating shield would show a better HFSN rejection because of its better tank  $Q$ .

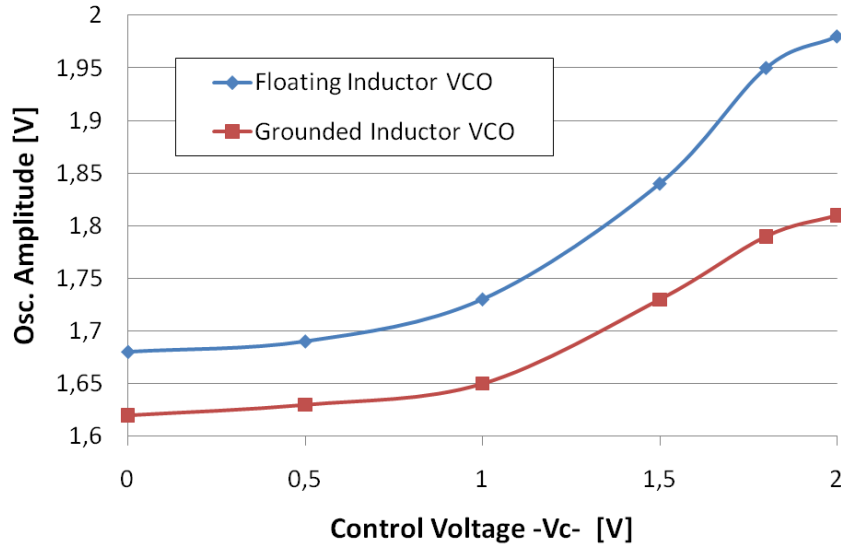


Figure 7.9. Oscillation amplitude of the grounded and floating VCOs.

### 7.4.3 Analysis of the oscillation frequency

The oscillation frequency also appears in (5.48) but it is not expected to be a relevant differentiation parameter because of the very similar inductance values of the two inductors, shown in Table 7.1. Fig. 7.11 plots the simulated oscillation frequency of both VCOs. The grounded shield inductor VCO has a higher oscillation frequency due to the slightly lower inductance. Note that although there is an increased frequency difference as  $V_c$  increases, its relative importance is well below the relative differences observed for the other parameters  $Q$  and  $A_o$ , thus the oscillation frequency is not expected to be a determining factor for the different noise robustness of the VCOs.

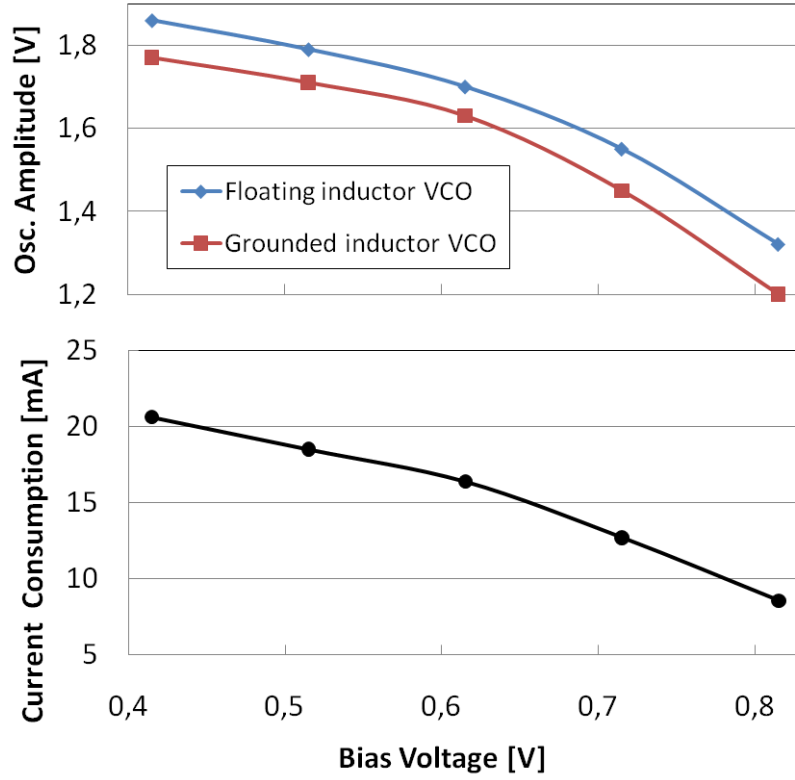


Figure 7.10. Relationship between oscillation amplitude, current consumption, and  $V_{bias}$  on the grounded and floating VCOs.

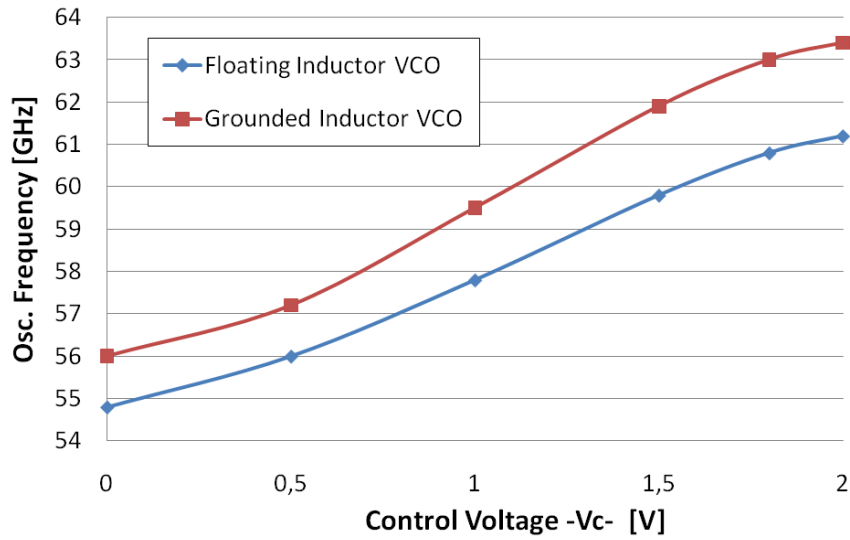


Figure 7.11. Oscillation frequency of the grounded and floating VCOs.

## 7.5 Model and simulation comparison

The analytical model of (5.48) together with the analysis of the different parameters has allowed deriving several conclusions regarding the noise immunity behavior of the VCOs to  $V_c$  and  $V_{bias}$ .

Both VCOs will behave similarly for low values of  $V_c$  where both VCO tanks have similar  $Q$  and oscillation amplitude. As  $V_c$  is increased, the robustness of the two VCOs will be improved but the improvement rate will be higher for the floating shield VCO than for the grounded shield VCO—the floating shield tank has significantly better  $Q$  and thus also better oscillation amplitude. On the contrary, similar improvement of the robustness to HFSN should be observed in both VCOs when the power consumption is increased.

The above qualitative conclusions derived from the observation of the model in (5.48) can be validated if the noise predicted by the model shows a close correlation with accurate simulations of the circuit, and further confirmed after experimental measurements of the two VCOs. This section details the verification of the model by comparing it against the noise levels obtained after detailed simulations of both VCOs. The values obtained from the  $Q$ ,  $A_o$  and  $\omega_o$  parameters as functions of  $V_c$  and  $V_{bias}$  are used in (5.48) to calculate the amplitude of the sideband spurs. Note that the  $A_i$  value—the noise amplitude in the tank—cannot be known from circuit simulations, thus it is arbitrarily set but assumed to be the same in both VCOs, in conformity with the assumption described in section 7.3. The model predictions obtained for a complete sweep of  $V_c$  are shown in Fig. 7.12, compared against the results of the circuit simulations described before in section 7.3. The comparison between the model and simulation results shows very good matching with an error less than 1 dB. The small difference between the simulation and the model results could be further reduced by taking into account the active elements of the design, together with their parasitics. Both the simulations and the model show that the difference of the sideband amplitudes between the VCOs is around 0.5 dB for the lowest  $V_c$  values, but increases to 2 dB at the highest  $V_c$ .

The prediction of the analytical model regarding the spur level as a function of the current consumption ( $V_{bias}$ ) is shown in Fig. 7.13, compared against the results obtained from the circuit simulation. Again, the model accurately predicts the results of the simulation. An increase in the power consumption—lower  $V_{bias}$ —produces an increase in the oscillation amplitude, thus improving the robustness of the VCOs to HFSN.

The agreement between the model predictions and the simulation results validates the proposed model for the purposes of predicting the amplitude of the sideband spurs produced by HFSN in mmW LC-VCOs.

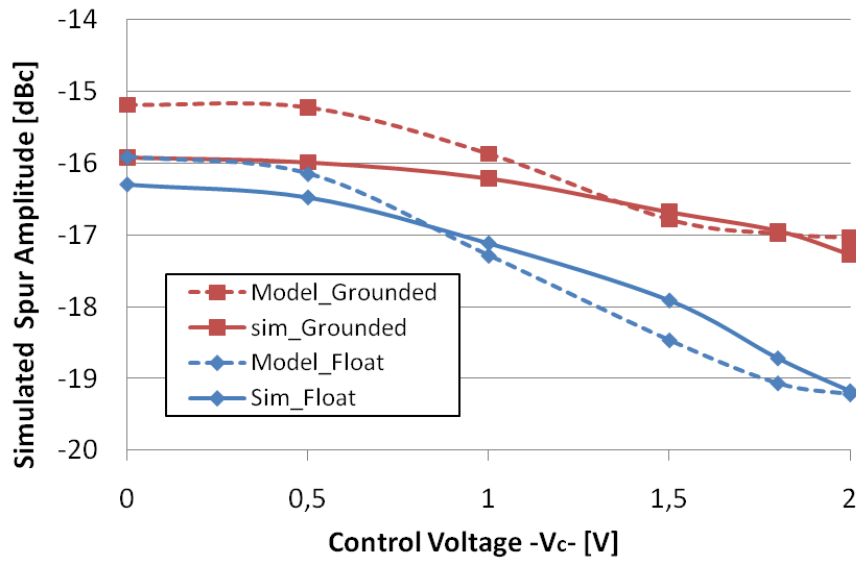


Figure 7.12. Relationship between  $V_c$  and the sideband spur amplitude predicted by model and simulation of both VCOs.

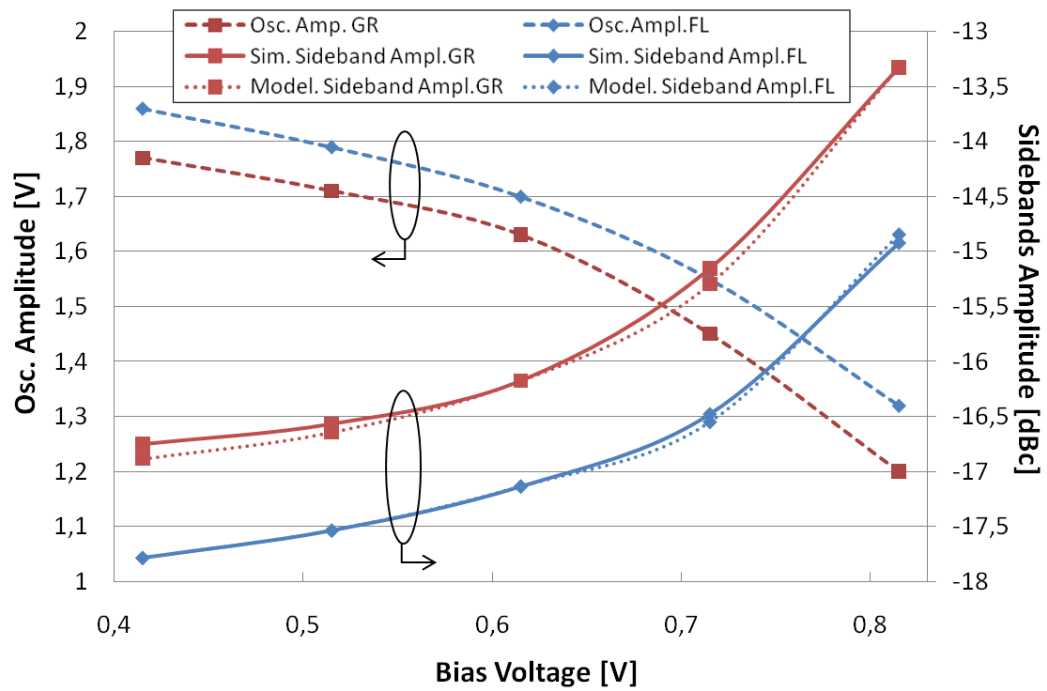


Figure 7.13. Relationship between oscillation amplitude and sideband amplitude predicted by model and simulation.

## 7.6 Experimental measurements of the effects of HFSN on mmW VCOs

The two VCOs under analysis were manufactured and used to experimentally characterize the effects of HFSN in terms of sideband spurs and thus validate the results of the analysis detailed in the

previous sections. The experiment consists in injecting a mmW noise tone directly into the substrate, with a frequency close to the oscillation of the VCO, and observe the effects on its output spectrum. To facilitate noise injection, an additional pad was included in the VCO layouts—see Fig. 7.3—which contacts the substrate through an array of P+ diffusion contacts. The measurements were done with the bare dies accessed with passive probes. Fig. 7.14 details the set-up of the measurements. The high gain of the LC-VCOs ( $10\text{ GHz/V}$ ) made measurements particularly challenging, being the precision and stability of the DC voltages a critical aspect to produce a stable output spectrum. A  $10\text{ dBm}$  noise tone is used in all the measurements, while different frequency offsets were selected.

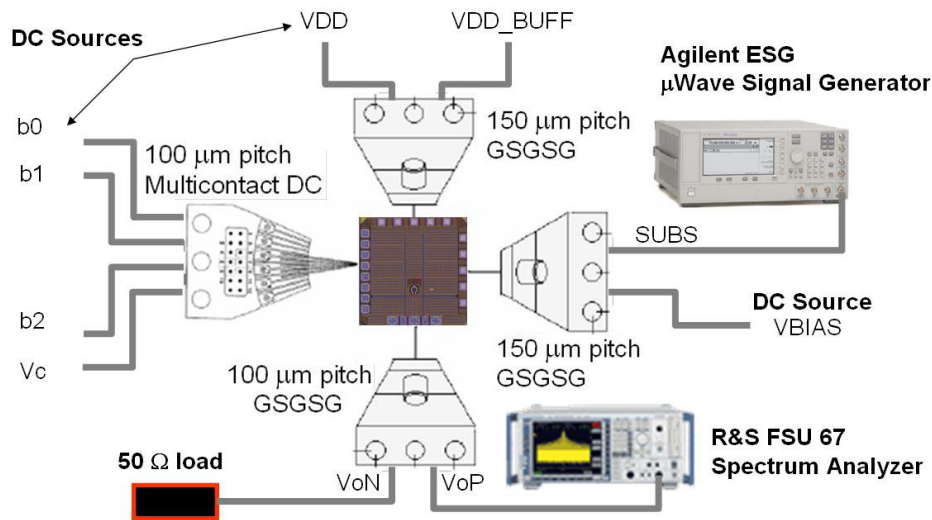


Figure 7.14. Scheme of the experimental set-up for the measurement of HFSN effects on the VCO output.

Fig. 7.15 shows the amplitude of the sideband spurs caused by the injected HFSN tone for two different values of  $V_c$  ( $V_c=0$  and  $V_c=1.8\text{ V}$ ) on the grounded shield and on the floating shield inductor VCOs. This measurement shows a  $20\text{ dB/dec}$  drop rate caused by the relationship between the frequency offset and the FM modulation index. The sideband spur amplitude for low values of  $V_c$  is higher and similar in both VCOs, as already predicted by the model and simulations. When switching  $V_c$  to its highest value, the spur level decreases in both cases, but the difference is significantly higher for the floating shield inductor VCO, suggesting a stronger dependence of the spur amplitude on  $V_c$  than is the case for the grounded shield inductor VCO.

A measurement of the amplitude of the spurs for a full sweep of  $V_c$  is shown in Fig. 7.16 and allows a better comparison to the model and simulation predictions shown in Fig. 7.12. Note that in this case a sweep of  $V_c$  produces different oscillation frequencies and amplitudes, which results in a significant variability of the measured relative sideband spur. A best fit line has been added

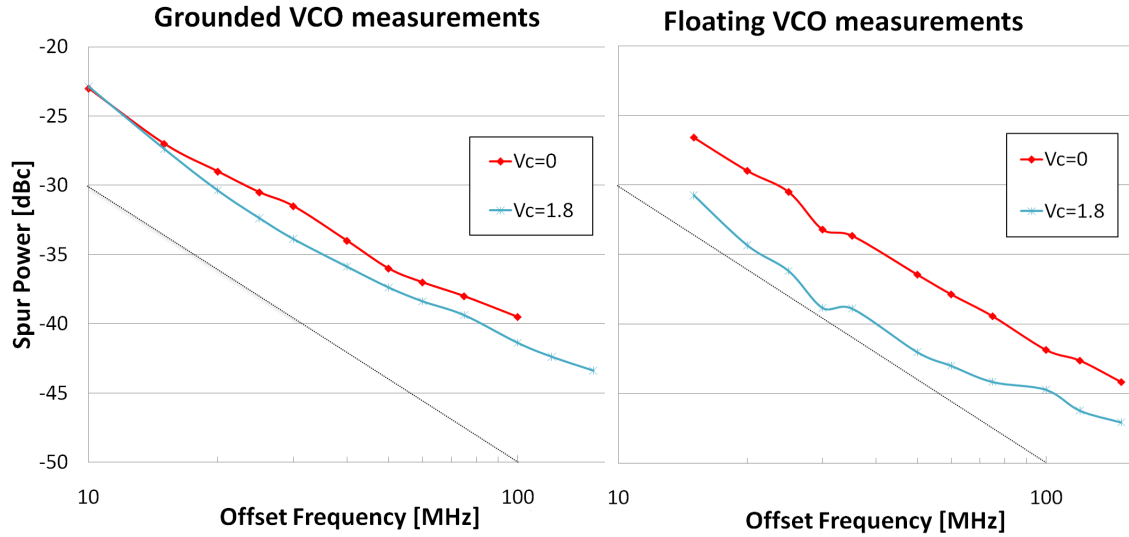


Figure 7.15. Measured sideband relative amplitudes for different frequency offsets.

to Fig. 7.16 to cope with this variability. The averaged behavior agrees reasonably well with the simulation and model predictions.

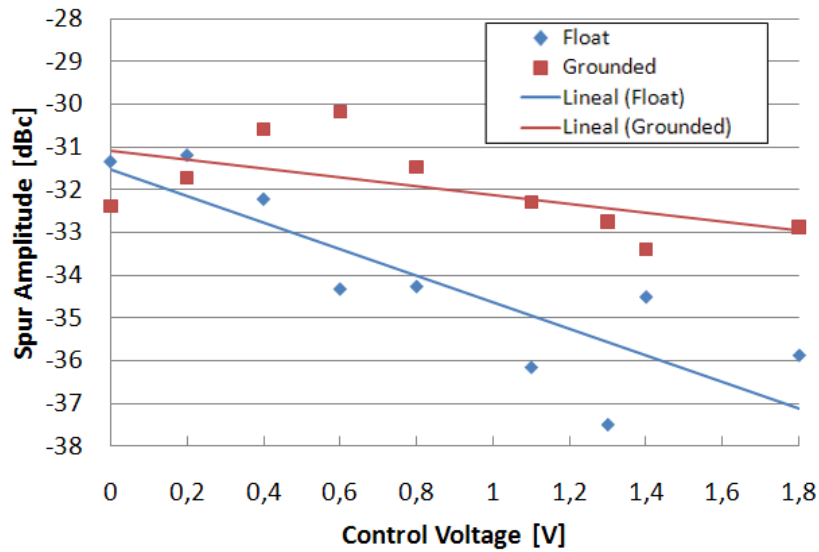


Figure 7.16. Measured spur amplitude for the grounded and floating VCOs

The relationship between the oscillation amplitude and the spur amplitude has also been experimentally measured through their dependence on  $V_{bias}$ . Fig. 7.17 shows on the left axis the variation of the output amplitude of both VCOs (after the buffers) which follows the simulation results in Fig. 7.13. The right axis represents the sideband amplitude as a function of  $V_{bias}$ , and again agrees with the behavior predicted in Fig. 7.13. These measurements then confirm the inverse relationship between oscillation amplitude and spur level described by the analytical model.

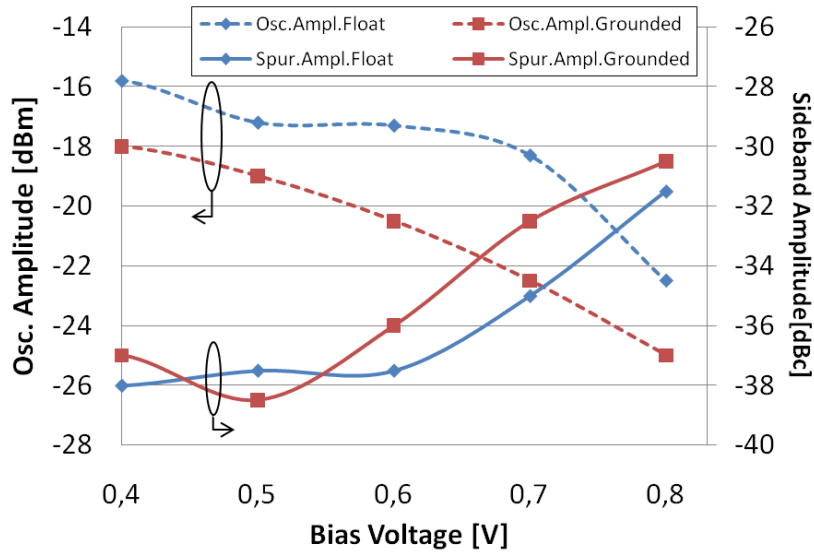


Figure 7.17. Comparison of the measured sideband amplitude with the oscillation amplitude.

The agreement between this set of measurements and the simulation and model predictions confirms the conclusions obtained in section 7.5 regarding the noise robustness of both VCOs and their dependence on the inductor characteristics. This further validates the assumption made in the simulations that the amount of noise reaching the tank can be considered the same in both VCOs despite the different shielding strategies used. Finally, it has been proven that the proposed analytical model proposed in chapter 5 is a useful tool for predicting and analyzing the behavior of a VCO under the effect of HFSN even at mmW frequencies.

## 7.7 Summary and conclusions

This chapter has presented the characterization of the effects of HFSN on LC-VCOs working in the mmWave frequencies. For that purpose, two 60 GHz LC-VCOs have been designed, identical except for the use of two different strategies to shield the inductor of the resonant tank. One of the inductors has a grounded patterned shield while the other has a floating patterned shield. The performed measurements have shown that the two oscillators have different level of degradation due to the HFSN.

The proposed model has been used to evaluate the HFSN robustness of the two millimeter wave LC-VCOs taking an important role to find the causes of the differences between the two oscillators.

The model faces two challenges in this analysis:



- Is the model still valid at the mmW frequency range?
- Can the model determine the cause of the different level of robustness to HFSN between the two LC-VCOs?

The carried analysis has concluded that the floating shield inductor increases the robustness of the LC-VCO to HFSN over the grounded shield inductor. In both cases, a very significant variation of the degradation has been measured when modifying the control voltage,  $V_c$ . The model states that the quality factor of the inductors, which in the floating shield is about 50% better than in the grounded shield, may have a strong correlation with the different level of robustness observed between both VCOs. The effect of the quality factor has also explained the effect of  $V_c$ . The control voltage  $V_c$  produces a strong variation in the varactor quality factor, which in turn produces variations in the overall  $Q$  of the tank, causing the degradation level differences as a function of  $V_c$ . The model has also shown that a better tank  $Q$  produces a double advantage in HFSN robustness. First, because of the higher oscillation amplitude and, secondly, because of the better  $Q$  itself.

The model has correctly determined the cause of the different level of robustness to HFSN between the two LC-VCOs. Measurements and simulation have supported the contributions of the model. The model has also shown that it is valid and accurate at the mmW frequency range.



## Chapter 8

# Conclusions.

This thesis has provided a model of the effect of the HFSN on LC-VCOs. A model that clearly identifies the main responsables of the oscillator degradation, showing the parameters of both, oscillator and noise, that should be addressed in order to increase the robustness of the oscillator. A lot of conclusions have arisen all along the process that has led to the presented model. These conclusions are summarized in this final chapter.

This thesis has started by empirically characterizing the propagation of noise through the substrate. The conclusions from this empirical investigation, together with the current state of the art analysis, have made apparent three reasons that justify the potential danger that the HFSN may represent: -The propagation of noise in the substrate is easier (less impedance) at high frequency than at low frequencies. -The measures to protect a victim from the noise in the substrate are much less efficient at high frequencies than at low frequencies -High frequency noise does not need a physical connection to reach the victim from the substrate, making the prediction of the coupling paths more difficult and increasing the number of point to protect.

A second analysis has been performed in order to empirically evaluate the potential danger that the HFSN may represent to the performance of an LC-VCO. A test LC-VCO has been manufactured including the possibility to inject noise in the substrate to test the effect of this noise in the oscillator performance. The analysis has concluded that HFSN can severely degrade the performance of an LC-VCO. The output of the oscillator is modulated in frequency due to the pulling effect of the HFSN. The HFSN perturbed LC-VCO behaves like an ILO that has lost the synchronization with the injected signal due to its small amplitude or to a high frequency offset between the oscillator and

the noise. The characteristics of the pulling effect can explain all the empirically found relationships between the degraded output spectrum and the HFSN and oscillator parameters.

The outcome of this empirical analysis together with the one presented before regarding the noise propagation lead to a clear conclusion which justifies the necessity of a deeper analysis on the effect of HFSN on LC-VCOs: High frequency noise can easily travel through the substrate and it can severely degrade the performance of the LC-VCO.

Thanks to the clear identification of the mechanism that causes the LC-VCO performance degradation provided by the empirical tests, it has been possible to define a particular analysis scenario in which an LC-VCO is pulled by a weak signal with a very similar frequency. This particular scenario reduces the high complexity of the methods to calculate the behavior of an unlocked ILO. A simple model has been developed that can accurately predict the effect of HFSN on LC-VCOs assuming that the limitations of the scenario are met. The accuracy of the model has been tested against 3 real LC-VCOs with different characteristics as well as against simulations. The evaluation has concluded that it is possible to accurately model the effect of HFSN on LC-VCOs with a model that is based in parameters of the oscillator and of the noise. In this case: Oscillation amplitude, oscillation frequency, tank quality factor, noise amplitude and frequency offset between oscillator and noise. The model is accurate at RF and at mmW frequency ranges.

The main advantage of having a model based on real parameters is that it exposes the points that should be addressed by a designer in order to reduce the performance degradation. The discussion around the model has also provided the trade offs and the consequences, or in other words: the price to pay, of implementing each of the measures arisen from the model. The concluded guidelines obtained from the model are summarized here:

- Tank quality factor: Increasing the tank quality factor increases the robustness of the oscillator. It is difficult to generalize a method to maximize the tank quality factor but it usually implies an investment in area or in extra wide metal layers.
- Oscillator amplitude: Increasing the oscillation amplitude increases the robustness of the oscillator. Power consumption is the most straight forward method to increase the oscillator amplitude. A CMOS topology provides double amplitude than NMOS or PMOS but increases transistor count, ie, area. Tank quality factor also impacts the oscillator amplitude.

- Oscillation frequency: The higher the oscillation frequency the higher the oscillator sensitivity. This is probably the least flexible design parameter for the designer as it is normally fixed.
- Noise amplitude: The amplitude of the noise that reaches the oscillator should be minimized. It has been concluded that substrate protection structures or distance between aggressor and victim may reduce the amount of noise reaching the oscillator. Area increase is an obvious consequence of these techniques.
- Frequency offset: The further away the oscillation frequency from the noise frequencies the less negative effects on the oscillator. Moving the LC-VCO frequency from the natural transceiver frequency usually involves a change at architectural level: frequency dividers, avoid zero or low IF, etc.

Following these rules provided by the model a designer may minimize the negative effects that HFSN has on the LC-VCO.

Some limitations of the proposed method have arisen during the presented analysis. These limitations also lead to some proposed future work.

- Where are the limits of validity of the model?

The fact of having obtained the proposed model from the combination of theory, measurement and simulation gives some confidence about its wide range of validity but the limits of this range of validity may be very difficult to define and may even differ from one LC-VCO to another. Two conditions were stated in the definition of the scenario where the model is valid, the noise amplitude must be much smaller than the oscillation amplitude and the noise frequency must be close to the free running oscillator frequency. Breaking any of these conditions may invalidate some of the presented rules. For example, if the noise frequency is very low it may cause an AM modulation of the output caused by the variable DC bias point of the tank. Also, if the noise amplitude is too high it may cause an strong pulling (which will invalidate the FM modulation assumption) or even locking. A deeper analysis of all the secondary possible effects (AM modulation, locking, intermodulation...) should be carried out to reliably define the model limitations.

- What is the effect of a degraded LC-VCO on a complete transceiver?

The complete presented analysis has treated the oscillator as an individual entity but in real

designs several other functional blocks work together with it. From a practical point of view, it is very important to understand the effect that the degraded signal of the oscillator may have on the complete transceiver. The first interesting area of analysis is the effect on a PLL. May the PLL reduce the signal degradation? under which conditions?.

Back at the beginning of this thesis an specific objective was stated: ”‘provide designers with models, design criteria and methodology to design LC-VCOs robust to high frequency substrate noise.’”. This thesis has provided a solid insight into the interaction between the HFSN and the LC-VCOs developing a model that has proven to be a useful tool to predict the behavior of the perturbed oscillator. The model has led to determine the required guidelines and design rules to increase the immunity of LC-VCOs to HFSN, fulfilling the presented objectives of this thesis.

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